Arria V Device Handbook

Volume 1: Device Overview and Datasheet

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Contents

Additional Information

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Chapter 1. Overview for the Arria V Device Family
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Chapter 2. Device Datasheet for Arria V Devices
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1. Overview for the Arria V Device Family

AV51001-1.1

Built on the 28-nm low-power process technology, Arria® V devices offer the lowest power and lowest system cost for mainstream applications. Arria V devices include unique innovations such as the lowest static power in its class, the lowest power transceivers of any midrange family, support for serial data rates up to 10.3125 gigabits per second (Gbps), a powerful collection of integrated hard intellectual property (IP), and a power-optimized core architecture, making Arria V devices ideal for the following applications:

- Power sensitive wireless infrastructure equipment
- 20G/40G bridging, switching, and packet processing applications
- High-definition video processing and image manipulation
- Intensive digital signal processing (DSP) applications

Arria V devices are available in the following variants:

- Arria V GX—FPGA with integrated 6-Gbps transceivers, this variant provides bandwidth, cost, and power levels that are optimized for high-volume data and signal-processing applications.
- Arria V GT—FPGA with integrated 10-Gbps transceivers, this variant provides enhanced high-speed serial I/O bandwidth for cost-sensitive data and signal processing applications.
- Arria V SX—system-on-a-chip (SoC) FPGA with integrated Arria V FPGA and ARM®-based hard processor system (HPS).
- Arria V ST—SoC FPGA with integrated Arria V FPGA, ARM-based HPS, and 10-Gbps transceivers.

The Arria V SoC FPGA variants feature an FPGA integrated with an HPS that consists of a dual-core ARM Cortex™-A9 MPCore™ processor, a rich set of peripherals, and a shared multiport SDRAM memory controller.

The unique feature set in Arria V devices was chosen to optimize power, cost, and performance. These features include a redesigned adaptive logic module (ALM), distributed memory, new 10-Kbit (M10K) internal memory blocks, variable-precision DSP blocks, and fractional clock synthesis phase-locked loops (PLLs) with a highly flexible clocking network, all interconnected by a power-optimized MultiTrack routing architecture.

Arria V devices provide interface support flexibility with up to 10-Gbps transceivers, 1.25-Gbps **LVDS**, 1.333-Gbps memory interfaces with low latency, and support for all mainstream single-ended and differential I/O standards, including 3.3 V. Arria V devices also offer the lowest system cost by requiring only three power rails to operate the devices and a thermal composite flip chip ball-grid array (BGA) packaging option. Arria V devices also support innovative features, such as configuration via protocol (CvP), partial reconfiguration, and design security.

Arria V devices provide the power, features, and cost you require to succeed with your designs. With these innovations, Arria V devices deliver ideal performance and capability for a wide range of applications.

Arria V Feature Summary

Table 1–1 lists the Arria V device features.

Table 1–1. Feature Summary for Arria V Devices (Part 1 of 3)

Feature	Details
Technology	■ 28-nm TSMC low-power process technology ■ Lowest static power in its class (less than 800 mW for 500 K logic elements (LEs) at 85°C junction under typical conditions) ■ 1.1-V core nominal voltage
Lowest-power serial transceivers of any midrange FPGA	■ 611-Mbps to 10.3125-Gbps integrated transceivers ■ Transmit pre-emphasis and receiver equalization ■ Dynamic reconfiguration of individual channels
FPGA General-purpose I/Os (GPIOs)	■ 1.25-Gbps **LVDS** ■ 667-MHz/1.333-Gbps external memory interface ■ On-chip termination (OCT) ■ 3.3-V support
Embedded transceiver hard IP	■ Custom implementation up to 10.3125 Gbps ■ PCI Express® (PCIe®) Gen1 and Gen2 ■ Gbps Ethernet (GbE) and XAUI physical coding sublayer (PCS) ■ Common Public Radio Interface (CPRI) PCS ■ Gigabit-capable passive optical network (GPON) PCS

Table 1–1. Feature Summary for Arria V Devices (Part 2 of 3)

Feature	Details
HPS (Arria V SX and ST devices only)	■ Dual-core ARM Cortex-A9 MPCore processor. Up to 800 MHz maximum frequency that supports symmetric and asymmetric multiprocessing ■ Interface peripherals—10/100/1000 Ethernet media access control (MAC), USB 2.0 On-The-Go (OTG) controller, Quad SPI flash controller, NAND flash controller, and SD/MMC/SDIO controller, UART, serial peripheral interface (SPI), I2C interfaces, and up to 86 GPIO interfaces ■ System peripherals—general-purpose and watchdog timers, direct memory access (DMA) controller, FPGA configuration manager, and clock and reset managers ■ On-chip RAM and boot ROM ■ HPS–FPGA bridges—include the FPGA-to-HPS, HPS-to-FPGA, and lightweight HPS-to-FPGA bridges that allow the FPGA fabric to master transactions to slaves in the HPS, and vice versa ■ FPGA-to-HPS SDRAM controller subsystem—provides a configurable interface to the multiport front end of the HPS SDRAM controller ■ ARM CoreSight™ JTAG debug, trace port, and on-chip trace storage ■ Three fractional PLLs
Physical medium attachment (PMA) with soft PCS	■ 10GBASE-R ■ 9.8304-Gbps CPRI
High-performance core fabric	■ Enhanced ALM with four registers ■ Improved routing architecture to reduce congestion and improve compilation time
Variable-precision DSP blocks	■ Natively supports three-signal processing precision ranging from 9 x 9, 18 x 19, or 27 x 27 in the same DSP block ■ 64-bit accumulator and cascade for systolic finite impulse responses (FIRs) ■ Embedded internal coefficient memory ■ Pre-adder/subtractor improves efficiency
Internal memory blocks	■ M10K, 10 Kbit with soft error correction code (ECC) ■ Memory logic array block (MLAB), 640-bit distributed LUTRAM—you can use up to 25% of the LEs as MLAB memory ■ Hardened double data rate3 (DDR3) and DDR2 memory controllers
High-resolution Fractional PLLs	■ Integer mode and fractional mode ■ Precision clock synthesis, clock delay compensation, and zero delay buffering (ZDB)
Clock networks	■ 625-MHz global clock network ■ Global, quadrant, and peripheral clock networks ■ Unused clock networks can be powered down to reduce dynamic power

Table 1–1. Feature Summary for Arria V Devices (Part 3 of 3)

Feature	Details
Configuration	■ Partial and dynamic reconfigurations ■ CvP ■ Configuration via HPS ■ Serial and parallel flash interface ■ Enhanced advanced encryption standard (AES) design security features ■ Tamper protection ■ Remote system upgrade
Packaging	■ Thermal composite flip chip BGA packaging ■ Multiple device densities with identical package footprints for seamless migration between different device densities ■ Lead, lead-free (Pb-free), and RoHS-compliant options

Arria V Family Plan

Arria V devices offer various thermal composite flip chip BGA packaging options with differing price and performance points. Table 1–2 and Table 1–3 list the Arria V devices features.

Table 1–2. Maximum Resource Counts for Arria V GX Devices

Feature	Arria V GX Device							
	5AGXA1	5AGXA3	5AGXA5	5AGXA7	5AGXB1	5AGXB3	5AGXB5	5AGXB7
ALMs	28,302	56,100	71,698	91,680	113,208	136,880	158,491	190,240
LE (K)	75	148.67	190	242.95	300	362.73	420	504.14
M10K memory blocks	800	1,051	1,180	1,366	1,510	1,726	2,054	2,414
MLAB memory (Kbit)	463	873	1,173	1,448	1,852	2,098	2,532	2,906
Block memory (KByte)	8,000	10,510	11,800	13,660	15,100	17,260	20,540	24,140
Variable-precision DSP blocks	240	396	600	800	920	1,045	1,092	1,156
18 x 19 multipliers	480	792	1,200	1,600	1,840	2,090	2,184	2,312
Fractional PLLs (1)	10	10	12	12	12	12	16	16
GPIO	480	480	544	544	704	704	704	704
LVDS transmitter (TX) (2)	68	68	120	120	160	160	156	160
LVDS receiver (RX) (2)	80	80	136	136	176	176	172	176
PCIe hard IP blocks	1	1	2	2	2	2	2	2
Hard memory controllers	2	2	4	4	4	4	4	4

Notes to Table 1–2:

(1) The total number of available fractional PLLs is a combination of general-purpose and transceiver PLLs. Transceiver fractional PLLs that are not used by the transceiver I/O can be used as general-purpose fractional PLLs.

(2) For the LVDS channels count for each package, refer to the *High-Speed Differential I/O Interfaces with DPA in Arria V Devices* chapter.

Table 1–3. Maximum Resource Counts for Arria V GT, SX, and ST Devices—*Preliminary*

Feature	Arria V GT Device		Arria V SX Device		Arria V ST Device	
	5AGTD3	5AGTD7	5ASXB3	5ASXB5	5ASTD3	5ASTD5
ALMs	136,880	190,240	132,075	174,340	132,075	174,340
LE (K)	362.73	504.14	350	462	350	462
M10K memory blocks	1,726	2,414	1,729	2,282	1,729	2,282
MLAB memory (Kb)	2,098	2,906	2,014	2,658	2,014	2,658
Block memory (KB)	17,260	24,140	17,288	22,820	17,288	22,820
Variable-precision DSP blocks	1,045	1,156	809	1,068	809	1,068
18 x 19 multipliers	2,090	2,312	1,618	2,186	1,618	2,186
FPGA Fractional PLLs (2)	12	16	TBD	TBD	TBD	TBD
HPS PLLs (2)	—	—	TBD	TBD	TBD	TBD
FPGA GPIO	704	704	528	528	528	528
HPS I/O	—	—	216	216	216	216
LVDS TX (1)	160	160	120	120	120	120
LVDS RX (1)	176	176	120	120	120	120
PCIe hard IP blocks	2	2	2	2	2	2
Hard memory controllers	4	4	3	3	3	3
HPS memory controllers	—	—	1	1	1	1
ARM Cortex–A9 MPCore processor	—	—	Dual-core	Dual-core	Dual-core	Dual-core

Notes to Table 1–3:

(1) For the LVDS channels count for each package, refer to the *High-Speed Differential I/O Interfaces with DPA in Arria V Devices* chapter.

(2) The total number of available fractional PLLs is a combination of general-purpose and transceiver PLLs. Transceiver fractional PLLs, when not used by the transceiver I/O, can be used as a general-purpose fractional PLL.

Table 1–4 lists the Arria V package plan. The package plan shows the GPIO counts, the maximum number of 6-Gbps transceivers available, and the maximum number of 10-Gbps transceivers available per density and package. Various combinations of 6-Gbps and 10-Gbps transceiver counts are available.

Table 1–4. Package Plan for Arria V Devices —*Preliminary* *(1)*

Varients	Devices	F672 (27 mm) Flip Chip		F896 (31 mm) Flip Chip			F1152 (35 mm) Flip Chip			F1517 (40 mm) Flip Chip		
		GPIO	XCVR	GPIO *(2)*	HPS I/O	XCVR	GPIO	HPS I/O	XCVR	GPIO	HPS I/O	XCVR
Arria V GX *(3)*	5AGXA1	336	9	480	—	12	—	—	—	—	—	—
	5AGXA3	336	9	480	—	12	—	—	—	—	—	—
	5AGXA5	336	9	384	—	18	544	—	24	—	—	—
	5AGXA7	336	9	384	—	18	544	—	24	—	—	—
	5AGXB1	—	—	384	—	18	544	—	24	704	—	24
	5AGXB3	—	—	384	—	18	544	—	24	704	—	24
	5AGXB5	—	—	—	—	—	544	—	24	704	—	36
	5AGXB7	—	—	—	—	—	544	—	24	704	—	36
Arria V GT *(4)*, *(5)*	5AGTD3	—	—	384	—	12, 2	544	—	12, 4	704	—	12, 4
	5AGTD7	—	—	—	—	—	544	—	12, 4	704	—	12, 8
Arria V SX *(3)*	5ASXB3	—	—	178	216	12	350	216	18	528	216	30
	5ASXB5	—	—	178	216	12	350	216	18	528	216	30
Arria V ST *(4)*, *(5)*	5ASTD3	—	—	178	216	6, 2	350	216	12, 2	528	216	12, 6
	5ASTD5	—	—	178	216	6, 2	350	216	12, 2	528	216	12, 6

Notes to Table 1–4:

(1) The arrows indicate the package vertical migration capability. Vertical migration allows you to migrate across device densities for devices having the same dedicated pins, configuration pins, and power pins for a given package.

(2) In the F896 package, the PCIe hard IP block on the right side of the 5AGXA5, 5AGXA7, 5AGXB1, 5AGXB3, and 5AGTD3 devices supports x1 for Gen1 and Gen2 data rates.

(3) The transceiver counts listed are for 6-Gbps transceivers.

(4) The transceiver counts listed are for 6-Gbps and 10-Gbps transceivers, respectively.

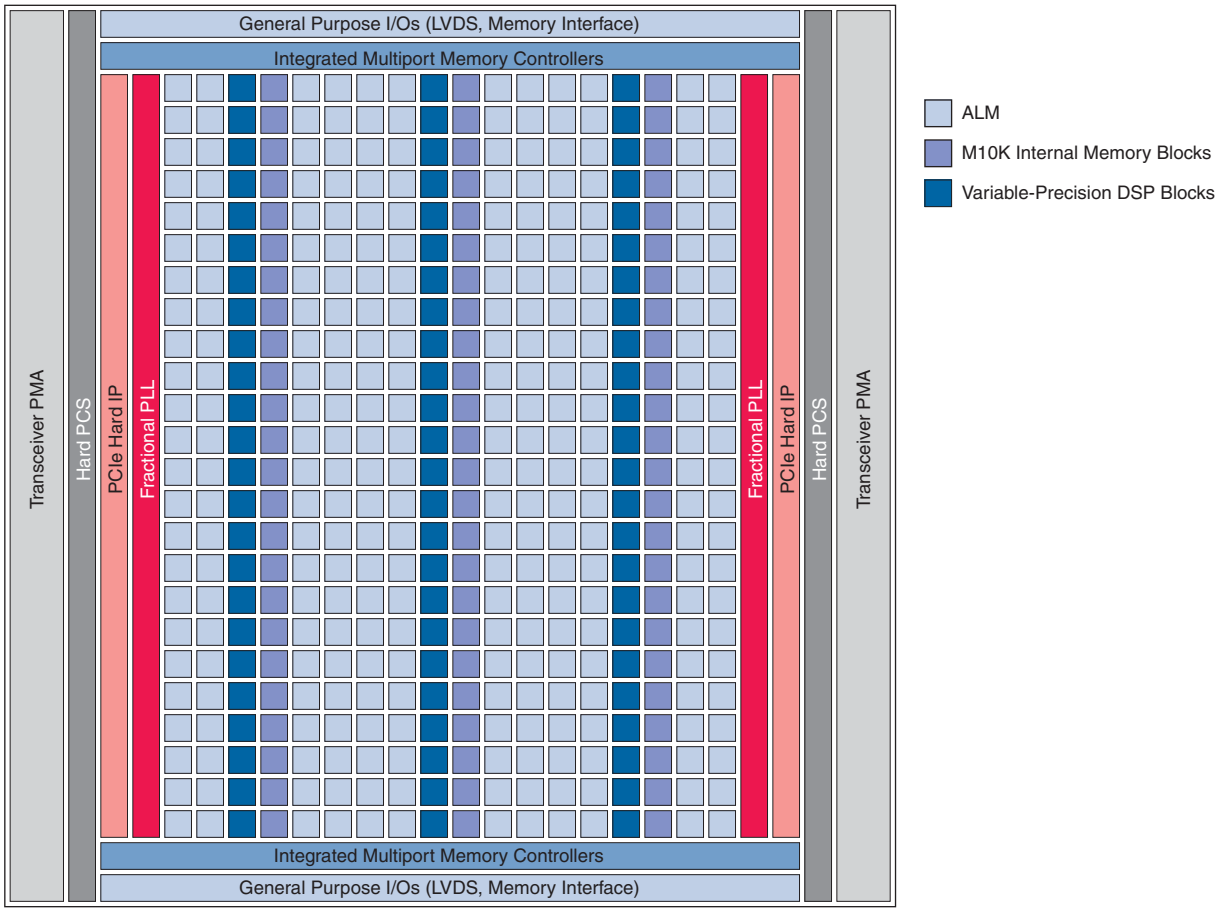
(5) You can alternatively configure any pair of 10-Gbps channels as six 6-Gbps channels. For instance, you can alternatively configure the 5AGTD7 device in the F1517 package as eighteen 6-Gbps and six 10-Gbps, twenty-four 6-Gbps and four 10-Gbps, or thirty 6-Gbps and two 10-Gbps channels.

Low-Power Serial Transceivers

Arria V devices deliver the industry's lowest power 10-Gbps transceivers at less than 140 mW and 6-Gbps transceivers at less than 100 mW power consumption per channel. Arria V transceivers are designed to be standard compliant for a wide range of protocols and data rates.

The transceivers are positioned on the left and right outer edges of the device, as shown in Figure 1–1.

Figure 1–1. Device Chip Overview for Arria V Devices *(1), (2)*



Notes to Figure 1–1:

(1) This figure represents an Arria V device with transceivers. Other Arria V devices may have a different floor plan than the one shown here.

(2) This figure is a graphical representation of a top view of the silicon die, which corresponds to a reverse view for flip chip packages.

PMA Support

To prevent core and I/O noise from coupling into the transceivers, the PMA block is isolated from the rest of the chip, ensuring optimal signal integrity. The transceiver channels consist of the PMA, PCS, and clock networks. You can also use the unused receiver PMA channels as additional transmit PLLs.

Table 1–5 lists the transceiver PMA features.

Table 1–5. Transceiver PMA Features for Arria V Devices

Features	Capability
Backplane support	Up to 16” FR4 PCB fabric drive capability at up to 6.5536 Gbps
Chip-to-chip support	Up to 10.3125 Gbps
PLL-based clock recovery	Superior jitter tolerance
Programmable serializer and deserializer (SERDES)	Flexible SERDES width
Equalization and pre-emphasis	Up to 6 dB of pre-emphasis and 4 dB of equalization
Ring oscillator transmit PLLs	611 Mbps to 10.3125 Gbps
Input reference clock range	27 MHz to 710 MHz
Transceiver dynamic reconfiguration	Allows reconfiguration of single channels without affecting operation of other channels

PCS Support

The Arria V core logic connects to the PCS through an 8-, 10-, 16-, 20-, 32-, or 40-bit interface, depending on the transceiver data rate and protocol. Arria V devices contain PCS hard IP to support PCIe Gen1 and Gen2, XAUI, GbE, Serial RapidIO® (SRIO), and CPRI protocols. All other standard and proprietary protocols from 611 Mbps to 6.5536 Gbps are supported through the custom double-width mode (up to 6.5536 Gbps) and custom single-width mode (up to 3.75 Gbps) transceiver PCS hard IP. A dedicated 80-bit interface to the core logic connects directly from the PMA, bypassing the PCS hard IP, to support all protocols beyond 6.5536 Gbps up to 10.3125 Gbps.

Table 1–6 lists the transceiver PCS features.

Table 1–6. Transceiver PCS Features for Arria V Devices (Part 1 of 2)

PCS Support (1)	Data Rates (Gbps)	Transmitter Data Path	Receiver Data Path
Custom single- and double-width modes	0.61 to ~6.5536	Phase compensation FIFO, byte serializer, and 8B/10B encoder	Word aligner, 8B/10B decoder, byte deserializer, and phase compensation FIFO
PCIe Gen1: x1, x2, x4, x8 PCIe Gen2: x1, x2, x4 (2)	2.5 and 5.0	The same as custom single- and double-width modes, plus PIPE 2.0 interface to the core logic	The same as custom single- and double-width modes, plus rate match FIFO and PIPE 2.0 interface to the core logic
GbE	1.25	The same as custom single- and double-width modes	The same as custom single- and double-width modes, plus rate match FIFO

Table 1–6. Transceiver PCS Features for Arria V Devices (Part 2 of 2)

PCS Support (1)	Data Rates (Gbps)	Transmitter Data Path	Receiver Data Path
XAUI	3.125	The same as custom single- and double-width modes, plus the XAUI state machine for bonding four channels	The same as custom single- and double-width modes, plus the XAUI state machine for realigning four channels, and deskew FIFO circuitry
SRIO	1.25 to 6.25	The same as custom single- and double-width modes	The same as custom single- and double-width modes
SDI	0.27 (3), 1.485, 2.97	Phase compensation FIFO, byte serializer	Byte deserializer and phase compensation FIFO
Serial ATA	1.5, 3.0, 6.0	Phase compensation FIFO, byte serializer, 8B/10B encoder	Phase compensation FIFO, byte deserializer, word aligner, and 8B/10B decoder
CPRI (4)	0.6144 to 6.144	The same as custom single- and double-width modes, plus the TX deterministic latency	The same as custom single- and double-width modes, plus the RX deterministic latency
GPON (5)	1.25 and 2.5	Phase compensation FIFO and byte serializer	Phase compensation FIFO and byte deserializer

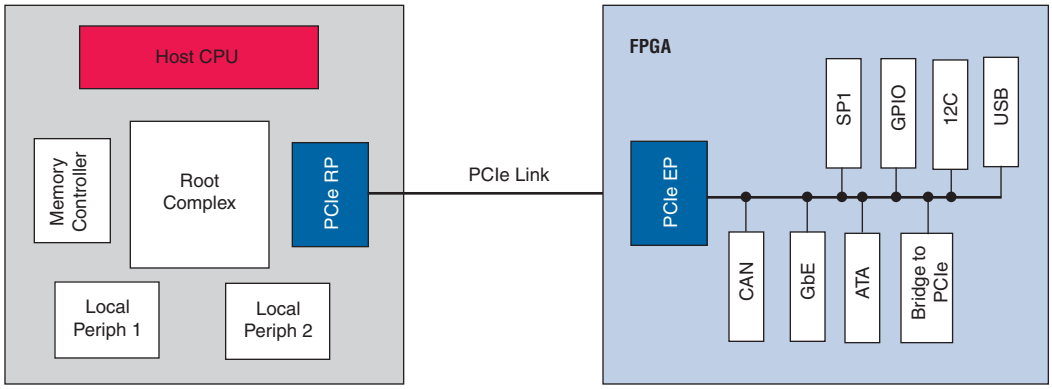
Notes to Table 1–6:

(1) Data rates above 6.5536 Gbps up to 10.3125 Gbps, such as 10GBASE-R, are supported through soft PCS.
(2) PCIe Gen2 is supported with the PCIe hard IP only.
(3) The 0.27-Gbps data rate is supported using oversampling user logics that you must implement in the FPGA fabric.
(4) CPRI data rates above 6.5536 Gbps, such as 9.8304 Gbps, are supported through soft PCS.
(5) The GPON standard does not support burst mode.

PCIe Gen1 and Gen2 Hard IP

Arria V devices contain PCIe hard IP designed for performance, ease-of-use, and increased functionality. The PCIe hard IP consists of the PHY MAC, data link, and transaction layers. The PCIe hard IP supports PCIe Gen2 end point and root port for up to x4 lane configurations, and PCIe Gen1 end point and root port for up to x8 lane configurations. PCIe endpoint support includes multifunction support for up to eight functions, as shown in Figure 1–2.

Figure 1–2. PCIe Multifunction for Arria V Devices



The Arria V PCIe hard IP operates independently from the core logic, which allows the PCIe link to wake up and complete link training in less than 100 ms, while the Arria V device completes loading the programming file for the rest of the device. In addition, the Arria V PCIe hard IP has improved end-to-end data path protection using ECC.

FPGA GPIOs

Arria V devices offer highly configurable GPIOs. The following list describes the many features of the GPIOs:

- Programmable bus hold and weak pull-up.
- **LVDS** output buffer with programmable differential output voltage (V_{OD}) and programmable pre-emphasis.
- Dynamic on-chip parallel termination (R_T OCT) for all I/O banks with OCT calibration to limit the termination impedance variation.
- On-chip dynamic termination to swap between serial and parallel termination, depending on whether there is reading or writing on a common bus for signal integrity.
- Configurable unused voltage reference (`VREF`) pins as user I/Os.
- Easy timing closure support using the hardened read FIFO in the input register path, and delay-locked loop (DLL) delay chain with fine and coarse architecture.

External Memory

Arria V devices support up to four hardened memory controllers for DDR3 and DDR2 SDRAM. Each controller supports 8- to 32-bit components up to 4 gigabits (Gb) in density with two-chip select and optional ECC. Arria V devices do not support DDR3 SDRAM leveling.

Arria V devices also support soft memory controllers for DDR3, DDR2, LPDDR2, and LPDDR SDRAM, RLDRAM II, QDR II, and QDR II+ SRAM for maximum flexibility.

Table 1–7 lists the external memory interface block performance.

Table 1–7. External Memory Interface Performance for Arria V Devices

Interface	Voltage (V)	Hard Controller (MHz)	Soft Controller (MHz)
DDR3 SDRAM	1.5	533	667
	1.35	533	667
	1.25	400	400
DDR2 SDRAM	1.8	400	400
	1.5	400	400
RLDRAM II	1.8	(1)	400
QDR II+ SRAM	1.8	(1)	400
	1.5	(1)	400
QDR II SRAM	1.8	(1)	400
	1.5	(1)	400
DDR II+ SRAM (2)	1.8	(1)	400
	1.5	(1)	400
LPDDR SDRAM (2)	1.8	(1)	200
LPDDR2 SDRAM (2)	1.2	(1)	400

Notes to Table 1–7:

(1) These memory interfaces are not supported in the hard memory controller.

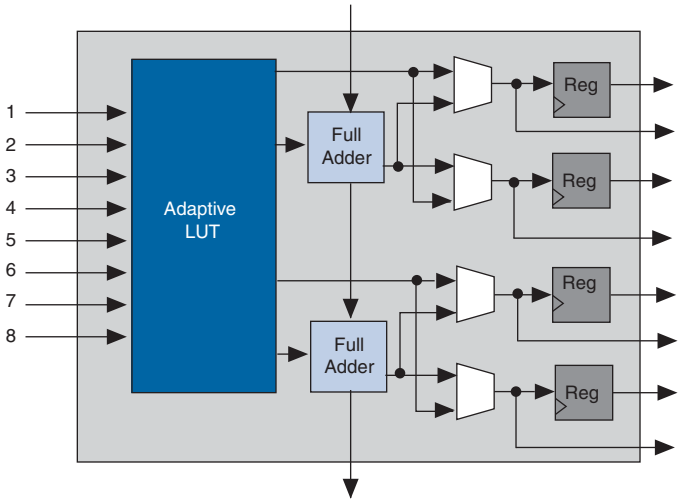
(2) These memory interfaces are not available as Altera® IP.

ALM

Arria V devices use a 28-nm ALM as the basic building block of the device fabric. The ALM shown in Figure 1–3 uses an 8-input fracturable look-up table (LUT) with four dedicated registers to help improve timing closure in register-rich designs and achieve an even higher design packing capability than previous generations.

You can configure up to 25% of the ALMs in Arria V devices as distributed MLABs. For more information, refer to "Embedded Memory" on page 1–14.

Figure 1–3. ALM for Arria V Devices



Variable-Precision DSP Block

Arria V devices feature a variable-precision DSP block that you can configure to support signal processing with precision ranging from 9 x 9, 18 x 19, and 27 x 27 bits natively.

You can independently configure each DSP block during compilation as a triple 9 x 9, a dual 18 x 19 multiply, or a single 27 x 27. With a dedicated 64-bit cascade bus, you can cascade multiple variable-precision DSP blocks to implement even higher precision DSP functions efficiently.

The variable precision DSP block also supports these features:

- 64-bit accumulator that is the largest in the industry,
- Double accumulator
- Hard pre-adder that is available in both 18- and 27-bit modes
- Cascaded output adders for efficient systolic FIR filters
- Dynamic coefficients
- 18-bit internal coefficient register banks
- Enhanced independent multiplier operation
- Efficient support for single floating point arithmetic
- Inferability of all modes by the Altera Complete Design Suite

Table 1–8 lists the accommodation of different configurations in a DSP block.

Table 1–8. Variable-Precision DSP Block Configurations for Arria V Devices

Multiplier Size (Bit)	DSP Block Resources	Expected Usage
Three 9 x 9	1 variable-precision DSP block	Low precision fixed point for video applications
Two18 x 19	1 of variable-precision DSP block	Medium precision fixed point in FIR filters
Two 18 x 19 with accumulate	1 variable-precision DSP block	FIR filters
One 27 x 27	1 variable-precision DSP block	Single precision floating point

Table 1–9 lists the number of multipliers in Arria V devices.

Table 1–9. Number of Multipliers in Arria V Devices

Variants	Devices	Variable Precision DSP Blocks	Independent Input and Output Multiplications Operator			18 x 19 Multiplier Adder Mode	18 x 18 Multiplier Adder Summed with 36-bit Input
			9 x 9 Multipliers	18 x 19 Multipliers	27 x 27 Multipliers		
Arria V GX	5AGXA1	240	720	480	240	240	240
	5AGXA3	396	1,188	792	396	396	396
	5AGXA5	600	1,800	1,200	600	600	600
	5AGXA7	800	2,400	1,600	800	800	800
	5AGXB1	920	2,760	1,840	920	920	920
	5AGXB3	1,045	3,135	2,090	1,045	1,045	1,045
	5AGXB5	1,092	3,276	2,184	1,092	1,092	1,092
	5AGXB7	1,139	3,417	2,278	1,139	1,139	1,139
Arria V GT	5AGTD3	1,045	3,135	2,090	1,045	1,045	1,045
	5AGTD7	1,139	3,417	2,278	1,139	1,139	1,139
Arria V SX	5ASXB3	809	2,427	1,618	809	809	809
	5ASXB5	1,068	3,204	2,136	1068	1,068	1,068
Arria V ST	5ASTD3	809	2,427	1,618	809	809	809
	5ASTD5	1,068	3,204	2,136	1068	1,068	1,068

Embedded Memory

The Arria V memory blocks are flexible and designed to provide an optimal amount of small- and large-sized memory arrays. Arria V devices contain two types of embedded memory blocks:

- 640-bit MLAB blocks—for wide and shallow memories. You can use up to 25% of the device LABs as MLAB. The MLAB operates at up to 500 MHz.
- 10-Kb M10K blocks—for larger memory configurations. The M10K embedded memory operates at up to 400 MHz.

Table 1–10 lists the supported memory configurations for Arria V devices.

Table 1–10. Embedded Memory Block Configuration for Arria V Devices

Memory Block	Depth (bits)	Programmable Widths
MLAB	32	x16, x18, or x20
M10K	256	x40 or x32
	512	x20 or x16
	1K	x10 or x8
	2K	x5 or x4
	4K	x2
	8K	x1

Dynamic and Partial Reconfiguration

Dynamic reconfiguration enables transceiver data rates or encoding schemes to be changed dynamically while maintaining data transfer on adjacent transceiver channels in Arria V devices. Dynamic reconfiguration is ideal for applications requiring on-the-fly multi-protocol or multi-rate support. You can reconfigure the PMA, PCS, and PCIe hard IP blocks with dynamic reconfiguration.

Partial reconfiguration allows you to reconfigure part of the device while other sections remain running. Partial reconfiguration is required in systems where the uptime is critical because it allows you to make updates or adjust functionality without disrupting other services. While lowering power and cost, partial reconfiguration also increases the effective logic density by removing the necessity to place the device functions that do not operate simultaneously. Instead, you can store these functions in external memory and load them as required. This reduces the size of the required device by allowing multiple applications on a single device, which saves board space and reduces power consumption.

Altera simplifies the time-intensive task of partial reconfiguration by building the partial reconfiguration capability on top of the proven incremental compile and design flow in the Quartus® II software. With this Altera solution, you do not need to know all the intricate device architecture details to perform a partial reconfiguration.

Partial reconfiguration is supported through the FPP x16 configuration interface. You can seamlessly use partial reconfiguration in tandem with dynamic reconfiguration to enable partial reconfiguration of both the core and transceiver simultaneously.

Clock Networks and PLL Clock Sources

The Arria V clock network architecture is based on Altera's proven global, quadrant, and peripheral clock structure, which is supported by dedicated clock input pins and fractional PLLs. Arria V devices have 16 global clock networks capable of up to 625 MHz operation. The Quartus II software identifies all unused sections of the clock network and powers them down, which reduces power consumption.

Arria V devices have up to 16 PLLs with 18 output counters per PLL. One fractional PLL can use up to 18 output counters and two adjacent fractional PLLs share the 18 output counters. You can use fractional PLLs to reduce the number of oscillators required on your board, as well as reduce the clock pins used in the device by synthesizing multiple clock frequencies from a single reference clock source. You can use the PLLs for frequency synthesis, on-chip clock deskew, jitter attenuation, dynamic phase-shift, zero delay buffers, counters reconfiguration, bandwidth reconfiguration, programmable output clock duty cycles, PLL cascading, and reference clock switchover.

Arria V devices use a fractional PLL architecture in addition to the historical integer PLL. When you use fractional PLL mode, you can use the PLLs for precision fractional-N frequency synthesis—removing the need for an off-chip reference clock. Transceiver fractional PLLs, when not used by the Transceiver I/O, can be used as general-purpose fractional PLLs by the FPGA fabric.

Enhanced Configuration and Configuration via Protocol

Arria V devices support 3.3-V programming voltage and the following configuration modes:

- active serial (AS)
- passive serial (PS)
- fast passive parallel (FPP)
- CvP
- Configuration via HPS
- configuration through JTAG

You can configure Arria V devices through PCIe using CvP instead of an external flash or ROM. The CvP mode offers the fastest configuration rate and flexibility with the easy-to-use PCIe hard IP block interface. The Arria V CvP implementation conforms to the PCIe 100-ms power-up-to-active time requirement.

For more information regarding CvP, refer to the *Configuration via Protocol (CvP) Implementation in Altera FPGAs User Guide*.

Table 1–11 lists the configuration modes that Arria V devices support.

Table 1–11. Configuration Modes and Features for Arria V Devices

Mode	Data Width (Bit)	Maximum Clock Rate (MHz)	Maximum Data Rate (Mbps)	Decompression	Design Security	Remote System Update	Partial Reconfiguration
AS	1, 4	100	—	✓	✓	✓	—
PS	1	125	125	✓	✓	—	—
FPP	8, 16	125	—	✓	✓	Parallel flash loader	16-bit only
CvP	x1, x2, x4, x8 (1)	—	—	✓	✓	✓	✓
HPS	32	125	—	✓	✓	Parallel flash loader	✓
JTAG	1	33	33	—	—	—	—

Note to Table 1–11:

(1) Number of lanes instead of bits.

Power Management

Arria V devices leverage FPGA architectural features and process technology advancements to reduce the total device core power consumption by as much as 50% when compared with Stratix IV devices at the same performance level.

Additionally, Arria V devices have a number of hard IP blocks that not only reduce logic resources but also deliver substantial power savings when compared with soft implementations. The list includes PCIe Gen1 and Gen2, XAUI, GbE, SRIO, GPON and CPRI protocols. The hard IP blocks consume up to 25% less power than equivalent soft implementations.

Arria V transceivers are also designed for power efficiency. As a result, the transceiver channels consume 50% less power than the previous generation of Arria devices.

SoC FPGA with HPS

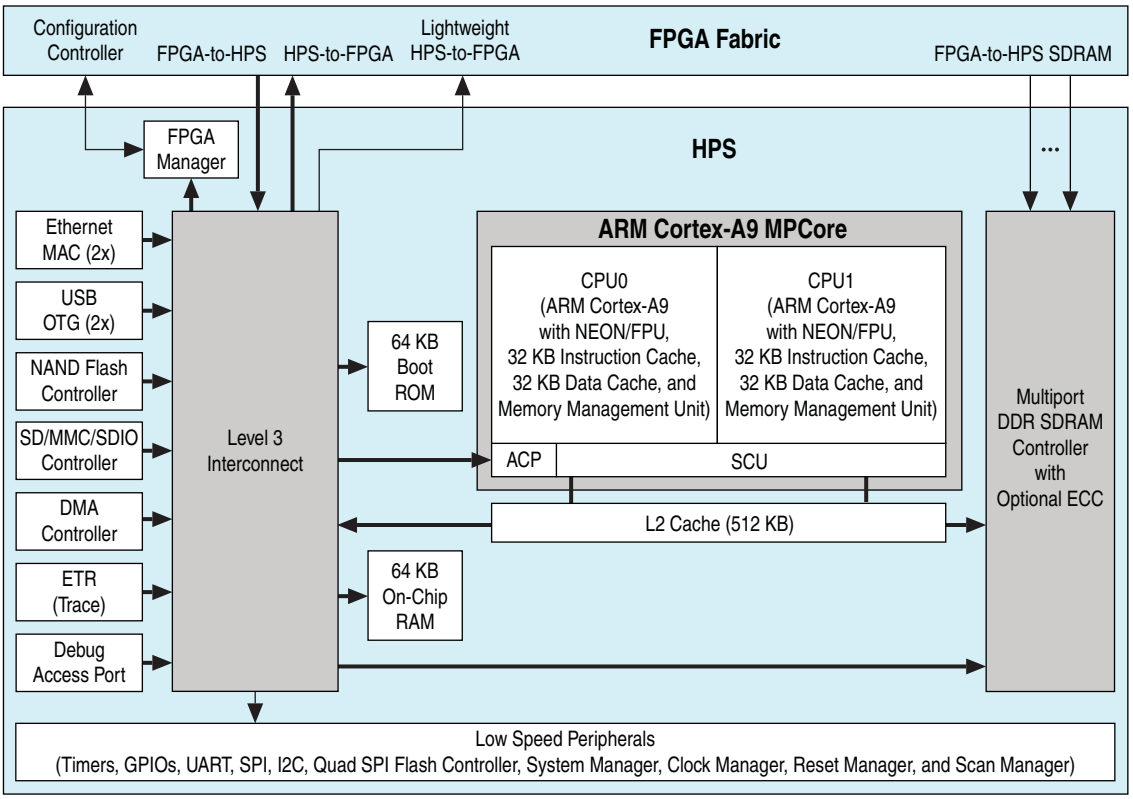
Each SoC FPGA device combines an FPGA fabric and an HPS in a single device. This combination delivers the flexibility of programmable logic with the power and cost savings of hard IP in the following ways:

- Reduces board space, system power, and bill of materials cost by eliminating a discrete embedded processor
- Allows you to differentiate the end product in both the hardware and software, and to support virtually any interface standard
- Extends the product life and revenue through in-field hardware and software updates

Features of the HPS

The HPS consists of a dual-core ARM Cortex-A9 MPCore processor, a rich set of peripherals, and a shared multiport SDRAM memory controller, as shown in Figure 1–4..

Figure 1–4. HPS with Dual-Core ARM Cortex-A9 MPCore Processor



System Peripherals

The Ethernet MAC, USB OTG controller, NAND flash controller and SD/MMC/SDIO controller modules have an integrated DMA controller. For modules without an integrated DMA controller, an additional DMA controller module provides up to eight channels for high-bandwidth data transfers. The debug access port provides interfaces to industry standard JTAG debug probes and supports ARM CoreSight debug and core traces to facilitate software development.

HPS-FPGA AXI Bridges

The HPS–FPGA bridges, which support the Advanced Microcontroller Bus Architecture (AMBA®) Advanced eXtensible Interface (AXI™) specifications, consist of the following bridges:

- FPGA-to-HPS AXI bridge—a high-performance bus supporting 32-, 64-, and 128-bit data widths that allows the FPGA fabric to master transactions to the slaves in the HPS
- HPS-to-FPGA AXI bridge—a high-performance bus supporting 32-, 64-, and 128-bit data widths that allows the HPS to master transactions to the slaves in the FPGA fabric.
- Lightweight HPS-to-FPGA AXI bridge—a lower performance 32-bit width bus that allows the HPS to master transactions to the slaves in the FPGA fabric.

The HPS–FPGA AXI bridges also allow the FPGA fabric to access the memory shared by one or both microprocessors, and provide asynchronous clock crossing with the clock from the FPGA fabric.

HPS SDRAM Controller Subsystem

The HPS SDRAM controller subsystem contains a multiport SDRAM controller and DDR PHY that is shared between the FPGA fabric (through the FPGA-to-HPS SDRAM interface), the level 2 (L2) cache, and the level 3 (L3) system interconnect. The FPGA-to-HPS SDRAM interface supports AMBA AXI and Avalon® Memory-Mapped (Avalon-MM) interface standards, and provides up to four ports with separate read and write directions.

To maximize memory performance, the HPS SDRAM controller subsystem supports command and data reordering, deficit round-robin arbitration with aging, and high-priority bypass features. The HPS SDRAM controller subsystem supports DDR2, DDR3, LPDDR, or LPDDR2 devices up to 4 Gb and runs up to 533 MHz (1066 Mbps data rate).

For easy migration, the FPGA-to-HPS SDRAM interface is compatible with the interface of the soft SDRAM memory controller IPs and hard SDRAM memory controllers in the FPGA fabric.

FPGA Configuration and Processor Booting

The FPGA fabric and HPS in the SoC FPGA are powered independently. You can reduce the clock frequencies or gate the clocks to reduce dynamic power, or shut down the entire FPGA fabric to reduce total system power.

You can configure the FPGA fabric and boot the HPS independently, in any order, providing you with more design flexibility:

- You can boot the HPS before you power up and configure the FPGA fabric. After the system is running, the HPS reconfigures the FPGA fabric at any time under program control or through the FPGA configuration controller.
- You can power up both the HPS and the FPGA fabric together, configure the FPGA fabric first, and then upload the boot code to the HPS from the FPGA fabric.

Hardware and Software Development

For hardware development, you can configure the HPS and connect your soft logic in the FPGA fabric to the HPS interfaces using the Qsys system integration tool in the Quartus II software.

For software development, the ARM-based SoC FPGA devices inherit the rich software development ecosystem available for the ARM Cortex-A9 MPCore processor. The software development process for Altera SoC FPGAs follows the same steps as those for other SoC devices. Altera also provides support for the Linux and VxWorks® operating systems.

You can begin device-specific firmware and software development on the Altera SoC FPGA Virtual Target. The Virtual Target is a PC-based fast-functional simulation of a target development system—a model of a complete development board that runs on a PC. The Virtual Target enables the development of device-specific production software that can run unmodified on actual hardware.

Ordering Information

This section describes the ordering information for Arria V devices.

Figure 1–5 and Figure 1–6 show the ordering codes for Arria V devices.

Figure 1–5. Ordering Information for Arria V GX and GT Devices

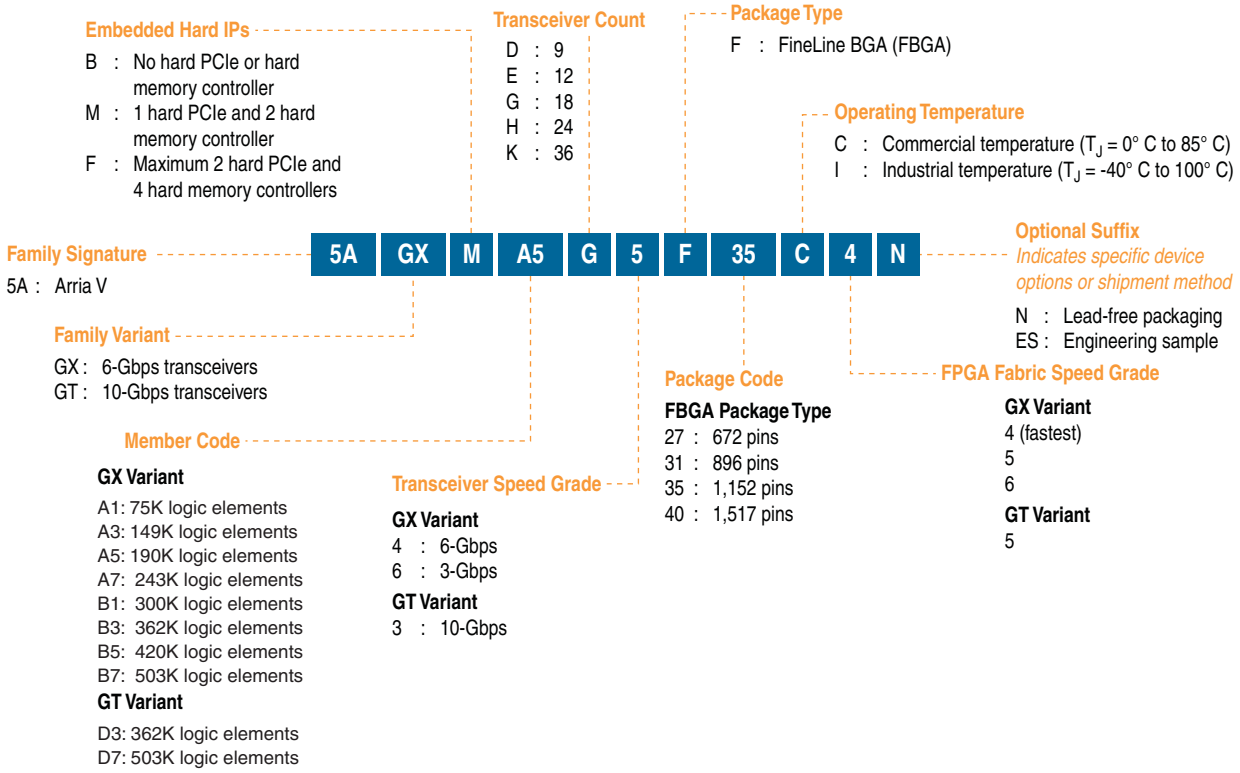
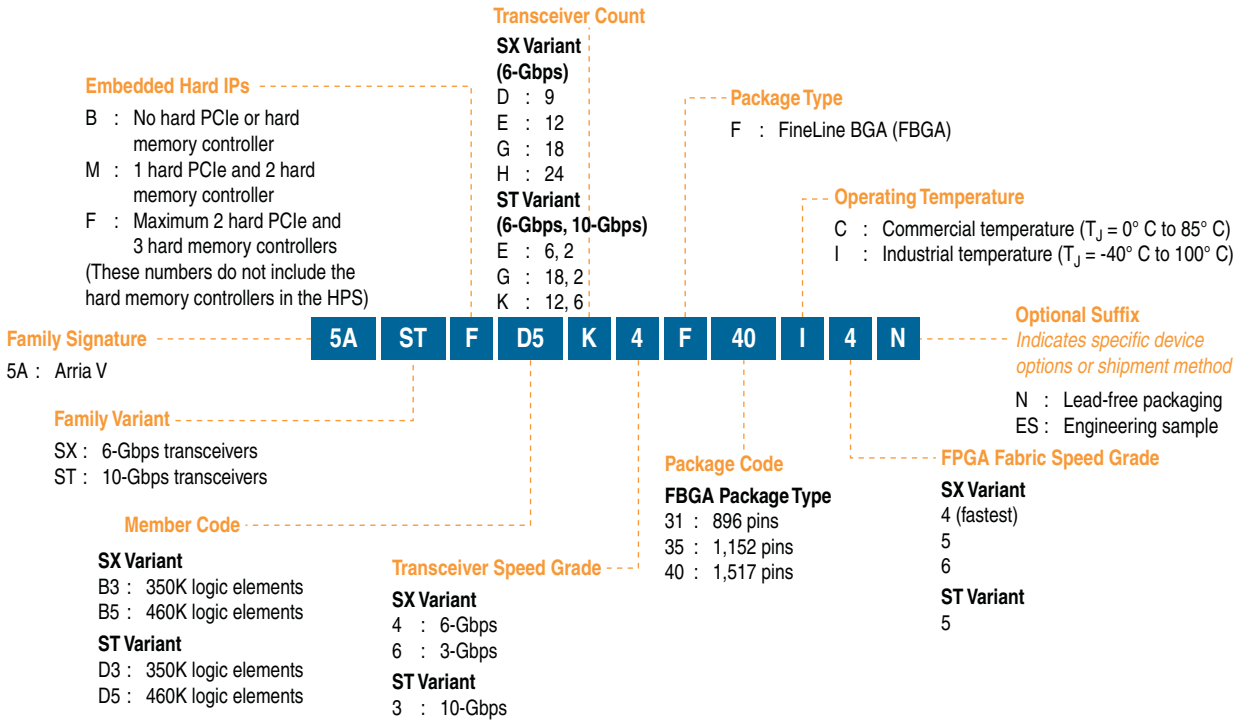


Figure 1–6. Ordering Information for Arria V SX and ST Devices



Document Revision History

Table 1–12 lists the revision history for this chapter.

Table 1–12. Document Revision History

Date	Version	Changes
November 2011	1.1	■ Updated Table 1–1, Table 1–2, Table 1–3, Table 1–4, Table 1–6, Table 1–7, Table 1–9, and Table 1–10. ■ Added "SoC FPGA with HPS" section. ■ Updated "Clock Networks and PLL Clock Sources" and "Ordering Information" sections. ■ Updated Figure 1–5. ■ Added Figure 1–6. ■ Minor text edits.
August 2011	1.0	Initial release.

2. Device Datasheet for Arria V Devices

AV-51002-1.1

This chapter describes the electrical characteristics, switching characteristics, and configuration specifications for Arria® V devices. Electrical characteristics include operating conditions and power consumption. Switching characteristics include transceiver specifications, and core and periphery performance. Configuration specifications include power-on reset (POR) specification, initialization clock source option and timing, various configuration mode timing parameters, remote system upgrades timing, and user watchdog internal oscillator frequency specification. This chapter also describes I/O timing, including programmable I/O element (IOE) delay and programmable output buffer delay.

For more information about the densities and packages of devices in the Arria V family, refer to the *Overview for Arria V Device Family* chapter.

Electrical Characteristics

The following sections describe the electrical characteristics of Arria V devices.

Operating Conditions

When you use Arria V devices, they are rated according to a set of defined parameters. To maintain the highest possible performance and reliability of the Arria V devices, you must consider the operating requirements described in this chapter.

Arria V devices are offered in commercial and industrial grades. Commercial devices are offered in –4 (fastest), –5, and –6 speed grades. Industrial grade devices are offered in the –5 speed grade.

Absolute Maximum Ratings

Absolute maximum ratings define the maximum operating conditions for Arria V devices. The values are based on experiments conducted with the devices and theoretical modeling of breakdown and damage mechanisms. The functional operation of the device is not implied for these conditions.

CAUTION

Conditions other than those listed in Table 2–1 may cause permanent damage to the device. Additionally, device operation at the absolute maximum ratings for extended periods of time may have adverse effects on the device.

Table 2–1. Absolute Maximum Ratings for Arria V Devices—*Preliminary*

Symbol	Description	Minimum	Maximum	Unit
V_{CC}	Core voltage and periphery circuitry power supply	–0.5	1.35	V
V_{CCPGM}	Configuration pins power supply	–0.5	3.75	V
V_{CCAUX}	Auxiliary supply	–0.5	3.75	V
V_{CCBAT}	Battery back-up power supply for design security volatile key register	–0.5	3.75	V
V_{CCPD}	I/O pre-driver power supply	–0.5	3.75	V
V_{CCIO}	I/O power supply	–0.5	3.9	V
V_{CCD_FPLL}	Phase-locked loop (PLL) digital power supply	–0.5	1.8	V
V_{CCA_FPLL}	PLL analog power supply	–0.5	3.75	V
V_{CCA_GXB}	Transceiver high voltage power	–0.5	3.75	V
V_{CCH_GXB}	Transmitter output buffer power	–0.5	1.8	V
V_{CCR_GXB}	Receiver power	–0.5	1.21	V
V_{CCT_GXB}	Transmitter power	–0.5	1.21	V
V_{CCL_GXB}	Clock network power	–0.5	1.21	V
V_I	DC input voltage	–0.5	4	V
I_{OUT}	DC output current per pin	–25	40	mA
T_J	Operating junction temperature	–55	125	°C
T_{STG}	Storage temperature (No bias)	–65	150	°C

Maximum Allowed Overshoot and Undershoot Voltage

During transitions, input signals may overshoot to the voltage listed in Table 2–2 and undershoot to –2.0 V for input currents less than 100 mA and periods shorter than 20 ns.

Table 2–2 lists the maximum allowed input overshoot voltage and the duration of the overshoot voltage as a percentage of device lifetime. The maximum allowed overshoot duration is specified as a percentage of high time over the lifetime of the device. A DC signal is equivalent to 100% duty cycle. For example, a signal that overshoots to 3.95 V can only be at 3.95 V for ~5% over the lifetime of the device; for a device lifetime of 10 years, this amounts to half a year.

Table 2–2. Maximum Allowed Overshoot During Transitions for Arria V Devices—*Preliminary*

Symbol	Description	Condition (V)	Overshoot Duration as % of High Time	Unit
Vi (AC)	AC input voltage	3.7	100	%
		3.75	59.79	%
		3.8	33.08	%
		3.85	18.45	%
		3.9	10.36	%
		3.95	5.87	%
		4	3.34	%
		4.05	1.92	%
		4.1	1.11	%

Recommended Operating Conditions

This section lists the functional operation limits for the AC and DC parameters for Arria V devices. Table 2–3 lists the steady-state voltage values expected from Arria V devices. Power supply ramps must all be strictly monotonic, without plateaus.

Table 2–3. Recommended Operating Conditions for Arria V Devices—*Preliminary* (Part 1 of 2)

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
V_{CC}	Core voltage and periphery circuitry power supply	—	1.07	1.1	1.13	V
V_{CCAUX}	Auxiliary supply	—	2.375	2.5	2.625	V
V_{CCPD} (1)	I/O pre-driver (3.3 V) power supply	—	3.135	3.3	3.465	V
	I/O pre-driver (3.0 V) power supply	—	2.85	3.0	3.15	V
	I/O pre-driver (2.5 V) power supply	—	2.375	2.5	2.625	V

Table 2–3. Recommended Operating Conditions for Arria V Devices—*Preliminary* (Part 2 of 2)

Symbol	Description	Condition	Minimum	Typical	Maximum	Unit
V_{CCIO}	I/O buffers (3.3 V) power supply	—	3.135	3.3	3.465	V
	I/O buffers (3.0 V) power supply	—	2.85	3.0	3.15	V
	I/O buffers (2.5 V) power supply	—	2.375	2.5	2.625	V
	I/O buffers (1.8 V) power supply	—	1.71	1.8	1.89	V
	I/O buffers (1.5 V) power supply	—	1.425	1.5	1.575	V
	I/O buffers (1.35 V) power supply	—	1.283	1.35	1.418	V
	I/O buffers (1.25 V) power supply	—	1.19	1.25	1.31	V
	I/O buffers (1.2 V) power supply	—	1.14	1.2	1.26	V
V_{CCPGM}	Configuration pins (3.3 V) power supply	—	3.135	3.3	3.465	V
	Configuration pins (3.0 V) power supply	—	2.85	3.0	3.15	V
	Configuration pins (2.5 V) power supply	—	2.375	2.5	2.625	V
	Configuration pins (1.8 V) power supply	—	1.71	1.8	1.89	V
V_{CCA_FPLL}	PLL analog voltage regulator power supply	—	2.375	2.5	2.625	V
V_{CCD_FPLL}	PLL digital voltage regulator power supply	—	1.425	1.5	1.575	V
V_{CCBAT} *(2)*	Battery back-up power supply (For design security volatile key register)	—	1.2	—	3.0	V
V_I	DC input voltage	—	–0.5	—	3.6	V
V_O	Output voltage	—	0	—	V_{CCIO}	V
T_J	Operating junction temperature	Commercial	0	—	85	°C
		Industrial	–40	—	100	°C
t_{RAMP} *(3)*	Power supply ramp time	Slow POR (PORSEL=0)	200 µs	—	100 ms	—
		Fast POR (PORSEL=1)	200 µs	—	4 ms	—

Notes to Table 2–3:

(1) V_{CCPD} must be 2.5 V when V_{CCIO} is 2.5, 1.8, 1.5, 1.35, 1.25 or 1.2 V. V_{CCPD} must be 3.0 V when V_{CCIO} is 3.0 V.

(2) If you do not use the design security feature in Arria V devices, connect V_{CCBAT} to a 1.5-V, 2.5-V or 3.0-V power supply. Arria V POR circuitry monitors V_{CCBAT}. Arria V devices do not exit POR if V_{CCBAT} stays low.

(3) When power is applied to an Arria V device, a POR occurs if the power supply reaches the recommended operating range in the maximum power supply ramp.

Table 2–4 lists the transceiver power supply recommended operating conditions for Arria V devices.

Table 2–4. Transceiver Power Supply Operating Conditions for Arria V GX and GT Devices—*Preliminary* (Part 1 of 2)

Symbol	Description	Minimum	Typical	Maximum	Unit
V_{CCA_GXBL}	Transceiver high voltage power (left side)	2.375	2.5	2.625	V
V_{CCA_GXBR}	Transceiver high voltage power (right side)				
V_{CCR_GXBL}	Receiver power (left side)	1.07	1.1	1.13	V
V_{CCR_GXBR}	Receiver power (right side)				
V_{CCT_GXBL}	Transmitter power (left side)	1.07	1.1	1.13	V
V_{CCT_GXBR}	Transmitter power (right side)				

Table 2–4. Transceiver Power Supply Operating Conditions for Arria V GX and GT Devices—*Preliminary* (Part 2 of 2)

Symbol	Description	Minimum	Typical	Maximum	Unit
V_{CCH_GXBL}	Transmitter output buffer power (left side)	1.425	1.5	1.575	V
V_{CCH_GXBR}	Transmitter output buffer power (right side)				
V_{CCL_GXBL}	Clock network power (left side)	1.07	1.1	1.13	V
V_{CCL_GXBR}	Clock network power (right side)	1.07	1.1	1.13	V

Table 2–5 lists the steady-state voltage and current values expected from Arria V system-on-a-chip (SoC) FPGA with ARM®-based hard processor system (HPS). Power supply ramps must all be strictly monotonic, without plateaus.

Table 2–5. HPS Power Supply Operating Conditions for Arria V Sx and ST Devices—*Preliminary*

Symbol	Description	Minimum	Typical	Maximum	Unit
V_{CC_HPS}	HPS Core voltage and periphery circuitry power supply	1.07	1.1	1.13	V
V_{CCPD_HPS}	HPS I/O pre-driver (3.3 V) power supply	3.135	3.3	3.465	V
	HPS I/O pre-driver (3.0 V) power supply	2.85	3.0	3.15	V
	HPS I/O pre-driver (2.5 V) power supply	2.375	2.5	2.625	V
V_{CCIO_HPS}	HPS I/O buffers (3.3 V) power supply	3.135	3.3	3.465	V
	HPS I/O buffers (3.0 V) power supply	2.85	3.0	3.15	V
	HPS I/O buffers (2.5 V) power supply	2.375	2.5	2.625	V
	HPS I/O buffers (1.8 V) power supply	1.71	1.8	1.89	V
	HPS I/O buffers (1.5 V) power supply	1.425	1.5	1.575	V
	HPS I/O buffers (1.2 V) power supply	1.14	1.2	1.26	V
$V_{CCRSTCLK\_HPS}$	HPS reset and clock input pins (3.3 V) power supply	3.135	3.3	3.465	V
	HPS reset and clock input pins (3.0 V) power supply	2.85	3.0	3.15	V
	HPS reset and clock input pins (2.5 V) power supply	2.375	2.5	2.625	V
	HPS reset and clock input pins (1.8 V) power supply	1.71	1.8	1.89	V
V_{CCPLL_HPS}	HPS PLL analog voltage regulator power supply	2.375	2.5	2.625	V

DC Characteristics

This section lists the supply current, I/O pin leakage current, input pin capacitance, on-chip termination tolerance, and hot socketing specifications.

Supply Current

Standby current is the current drawn from the respective power rails used for power budgeting. Use the Excel-based Early Power Estimator (EPE) to estimate supply current for your design because these currents vary greatly with the resources you use.

For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

I/O Pin Leakage Current

Table 2–6 lists the Arria V I/O pin leakage current specifications.

Table 2–6. I/O Pin Leakage Current for Arria V Devices—*Preliminary*

Symbol	Description	Conditions	Min	Typ	Max	Unit
I_I	Input pin	V_I = 0 V to $V_{CCIOMAX}$	–30	—	30	µA
I_{OZ}	Tri-stated I/O pin	V_O = 0 V to $V_{CCIOMAX}$	–30	—	30	µA

Bus Hold Specifications

Table 2–7 lists the Arria V device bus hold specifications.

Table 2–7. Bus Hold Parameters for Arria V Devices—*Preliminary* (1)

Parameter	Symbol	Conditions	V_{CCIO} (V)												Unit
			1.2		1.5		1.8		2.5		3.0		3.3		
			Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	
Bus-hold, low, sustaining current	I_{SUSL}	$V_{IN} > V_{IL}$ (max.)	8	—	12	—	30	—	50	—	70	—	70	—	µA
Bus-hold, high, sustaining current	I_{SUSH}	$V_{IN} < V_{IH}$ (min.)	–8	—	–12	—	–30	—	–50	—	–70	—	-70	—	µA
Bus-hold, low, overdrive current	I_{ODL}	$0V < V_{IN} < V_{CCIO}$	—	125	—	175	—	200	—	300	—	500	—	500	µA
Bus-hold, high, overdrive current	I_{ODH}	$0V < V_{IN} < V_{CCIO}$	—	-125	—	-175	—	-200	—	-300	—	-500	—	-500	µA
Bus-hold trip point	V_{TRIP}	—	0.3	0.9	0.375	1.125	0.68	1.07	0.7	1.7	0.8	2	0.8	2	V

Note to Table 2–7:

(1) The bus-hold trip points are based on calculated input voltages from the JEDEC standard.

(OCT) Specifications

If you enable on-chip termination (OCT) calibration, calibration is automatically performed at power up for I/Os connected to the calibration block. Table 2–8 lists the Arria V OCT termination calibration accuracy specifications.

Table 2–8. OCT Calibration Accuracy Specifications for Arria V Devices—*Preliminary* (1)

Symbol	Description	Conditions (V)	Calibration Accuracy			Unit
			C4	C5, I5	C6	
25-Ω R_S	Internal series termination with calibration (25-Ω setting)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2	±15	±15	±15	%
50-Ω R_S	Internal series termination with calibration (50-Ω setting)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2	±15	±15	±15	%
34-Ω and 40-Ω R_S	Internal series termination with calibration (34-Ω and 40-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25, 1.2	±15	±15	±15	%
48-Ω, 60-Ω, and 80-Ω R_S	Internal series termination with calibration (48-Ω, 60-Ω, and 80-Ω setting)	V_{CCIO} = 1.2	±15	±15	±15	%
50-Ω R_T	Internal parallel termination with calibration (50-Ω setting)	V_{CCIO} = 2.5, 1.8, 1.5, 1.2	–10 to +40	–10 to +40	–10 to +40	%
20-Ω, 30-Ω, 40-Ω,60-Ω, and 120-Ω R_T	Internal parallel termination with calibration (20-Ω, 30-Ω, 40-Ω, 60-Ω, and 120-Ω setting)	V_{CCIO} = 1.5, 1.35, 1.25	–10 to +40	–10 to +40	–10 to +40	%
60-Ω and 120-Ω R_T	Internal parallel termination with calibration (60-Ω and 120-Ω setting)	V_{CCIO} = 1.2	–10 to +40	–10 to +40	–10 to +40	%
25-Ω $R_{S\_left\_shift}$	Internal left shift series termination with calibration (25-Ω $R_{S\_left\_shift}$ setting)	V_{CCIO} = 3.0, 2.5, 1.8, 1.5, 1.2	±15	±15	±15	%

Note to Table 2–8:

(1) OCT calibration accuracy is valid at the time of calibration only.

Calibration accuracy for the calibrated on-chip series termination (R_S OCT) and on-chip parallel termination (R_T OCT) are applicable at the moment of calibration. When process, voltage, and temperature (PVT) conditions change after calibration, the tolerance may change.

Table 2–9 lists the Arria V OCT without calibration resistance tolerance to PVT changes.

Table 2–9. OCT Without Calibration Resistance Tolerance Specifications for Arria V Devices—*Preliminary*

Symbol	Description	Conditions (V)	Resistance Tolerance			Unit
			C4	C5, I5	C6	
25-Ω R_S	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 3.0 and 2.5	±30	±40	±40	%
25-Ω R_S	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 1.8 and 1.5	±30	±40	±40	%
25-Ω R_S	Internal series termination without calibration (25-Ω setting)	V_{CCIO} = 1.2	±35	±50	±50	%
50-Ω R_S	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 3.0 and 2.5	±30	±40	±40	%
50-Ω R_S	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.8 and 1.5	±30	±40	±40	%
50-Ω R_S	Internal series termination without calibration (50-Ω setting)	V_{CCIO} = 1.2	±35	±50	±50	%
100-Ω R_D	Internal differential termination (100-Ω setting)	V_{CCIO} = 2.5	±25	TBD	TBD	%

OCT calibration is automatically performed at power up for OCT-enabled I/Os. Table 2–10 lists OCT variation with temperature and voltage after power-up calibration. Use Table 2–10 to determine the OCT variation after power-up calibration and Equation 2–1 to determine the OCT variation without recalibration.

Equation 2–1. OCT Variation Without Recalibration—*Preliminary* *(1), (2), (3), (4), (5), (6)*

$$R_{OCT} = R_{SCAL}\left(1 + \langle\frac{dR}{dT} \times \Delta T\rangle \pm \langle\frac{dR}{dV} \times \Delta V\rangle\right)$$

Notes to Equation 2–1:

(1) The R_{OCT} value calculated from Equation 2–1 shows the range of OCT resistance with the variation of temperature and V_{CCIO}.
(2) R_{SCAL} is the OCT resistance value at power-up.
(3) ΔT is the variation of temperature with respect to the temperature at power up.
(4) ΔV is the variation of voltage with respect to the V_{CCIO} at power up.
(5) dR/dT is the percentage change of R_{SCAL} with temperature.
(6) dR/dV is the percentage change of R_{SCAL} with voltage.

Table 2–10 lists the OCT variation after the power-up calibration.

Table 2–10. OCT Variation after Power-Up Calibration for Arria V Devices—*Preliminary* (1)

Symbol	Description	V_{CCIO} (V)	Value	Unit
dR/dV	OCT variation of voltage without recalibration	3.0	0.0297	%/mV
		2.5	0.0344	
		1.8	0.0499	
		1.5	0.0744	
		1.2	0.1241	
dR/dT	OCT variation of temperature without recalibration	3.0	0.189	%/°C
		2.5	0.208	
		1.8	0.266	
		1.5	0.273	
		1.2	0.317	

Note to Table 2–10:

(1) Valid for a V_{CCIO} range of ±5% and temperature range of 0° to 85°C.

Pin Capacitance

Table 2–11 lists the Arria V pin capacitance.

Table 2–11. Pin Capacitance for Arria V Devices

Symbol	Description	Value	Unit
C_{IOTB}	Input capacitance on top/bottom I/O pins	5.5	pF
C_{IOLR}	Input capacitance on left/right I/O pins	5.5	pF
C_{OUTFB}	Input capacitance on dual-purpose clock output/feedback pins	5.5	pF

Hot Socketing

Table 2–12 lists the hot socketing specifications for Arria V devices.

Table 2–12. Hot Socketing Specifications for Arria V Devices—*Preliminary*

Symbol	Description	Maximum
$I_{IOPIN\ (DC)}$	DC current per I/O pin	300 µA
$I_{IOPIN\ (AC)}$	AC current per I/O pin	8 mA (1)
$I_{XCVR\text{-}TX\ (DC)}$	DC current per transceiver transmitter (TX) pin	100 mA
$I_{XCVR\text{-}RX\ (DC)}$	DC current per transceiver receiver (RX) pin	50 mA

Note to Table 2–12:

(1) The I/O ramp rate is 10 ns or more. For ramp rates faster than 10 ns, $|I_{IOPIN}| = C\ dv/dt$, in which C is the I/O pin capacitance and dv/dt is the slew rate.

Internal Weak Pull-Up Resistor

Table 2–13 lists the weak pull-up resistor values for Arria V devices.

Table 2–13. Internal Weak Pull-Up Resistor Values for Arria V Devices—*Preliminary* (1), (2)

Symbol	Description	Conditions (V) (3)	Value (4)	Unit
R_{PU}	Value of the I/O pin pull-up resistor before and during configuration, as well as user mode if you have enabled the programmable pull-up resistor option.	V_{CCIO} = 3.3 ±5%	25	kΩ
		V_{CCIO} = 3.0 ±5%	25	kΩ
		V_{CCIO} = 2.5 ±5%	25	kΩ
		V_{CCIO} = 1.8 ±5%	25	kΩ
		V_{CCIO} = 1.5 ±5%	25	kΩ
		V_{CCIO} = 1.35 ±5%	25	kΩ
		V_{CCIO} = 1.25 ±5%	25	kΩ
		V_{CCIO} = 1.2 ±5%	25	kΩ

Notes to Table 2–13:

(1) All I/O pins have an option to enable weak pull-up except the configuration, test, and JTAG pins.

(2) The internal weak pull-down feature is only available for the JTAG TCK pin. The typical value for this internal weak pull-down resistor is approximately 25 kΩ.

(3) Pin pull-up resistance values may be lower if an external source drives the pin higher than V_{CCIO}.

(4) Valid with ±10% tolerances to cover changes over PVT.

I/O Standard Specifications

Table 2–14 through Table 2–19 list the input voltage (V_{IH} and V_{IL}), output voltage (V_{OH} and V_{OL}), and current drive characteristics (I_{OH} and I_{OL}) for various I/O standards supported by Arria V devices. The I/O standards tables also list the Arria V device family I/O standard specifications. The V_{OL} and V_{OH} values are valid at the corresponding I_{OH} and I_{OL}, respectively.

For an explanation of terms used in Table 2–14 through Table 2–19, refer to "Glossary" on page 2–47.

Table 2–14. Single-Ended I/O Standards for Arria V Devices—*Preliminary* (Part 1 of 2)

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
3.3-V LVTTL	3.135	3.3	3.465	–0.3	0.8	1.7	3.6	0.45	2.4	4	–4
3.3-V LVCMOS	3.135	3.3	3.465	–0.3	0.8	1.7	3.6	0.2	V_{CCIO} – 0.2	2	–2
3.0-V LVTTL	2.85	3	3.15	–0.3	0.8	1.7	3.6	0.4	2.4	2	–2
3.0-V LVCMOS	2.85	3	3.15	–0.3	0.8	1.7	3.6	0.2	V_{CCIO} – 0.2	0.1	–0.1
3.0-V PCI	2.85	3	3.15	—	0.3 x V_{CCIO}	0.5 x V_{CCIO}	V_{CCIO} + 0.3	0.1 x V_{CCIO}	0.9 x V_{CCIO}	1.5	–0.5
3.0-V PCI-X	2.85	3	3.15	—	0.35 x V_{CCIO}	0.5 x V_{CCIO}	V_{CCIO} + 0.3	0.1 x V_{CCIO}	0.9 x V_{CCIO}	1.5	–0.5
2.5 V	2.375	2.5	2.625	–0.3	0.7	1.7	3.6	0.4	2	1	–1
1.8 V	1.71	1.8	1.89	–0.3	0.35 x V_{CCIO}	0.65 x V_{CCIO}	V_{CCIO} + 0.3	0.45	V_{CCIO} – 0.45	2	–2

Table 2–14. Single-Ended I/O Standards for Arria V Devices—*Preliminary* (Part 2 of 2)

I/O Standard	V_{CCIO} (V)			V_{IL} (V)		V_{IH} (V)		V_{OL} (V)	V_{OH} (V)	I_{OL} (mA)	I_{OH} (mA)
	Min	Typ	Max	Min	Max	Min	Max	Max	Min		
1.5 V	1.425	1.5	1.575	–0.3	0.35 x V_{CCIO}	0.65 x V_{CCIO}	V_{CCIO} + 0.3	0.25 x V_{CCIO}	0.75 x V_{CCIO}	2	–2
1.2 V	1.14	1.2	1.26	–0.3	0.35 x V_{CCIO}	0.65 x V_{CCIO}	V_{CCIO} + 0.3	0.25 x V_{CCIO}	0.75 x V_{CCIO}	2	–2

Table 2–15. Single-Ended SSTL and HSTL I/O Reference Voltage Specifications for Arria V Devices—*Preliminary*

I/O Standard	V_{CCIO}(V)			V_{REF}(V)			V_{TT}(V)		
	Min	Typ	Max	Min	Typ	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.49 x V_{CCIO}	0.5 x V_{CCIO}	0.51 x V_{CCIO}	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
SSTL-18 Class I, II	1.71	1.8	1.89	0.833	0.9	0.969	V_{REF} – 0.04	V_{REF}	V_{REF} + 0.04
SSTL-15 Class I, II	1.425	1.5	1.575	0.49 x V_{CCIO}	0.5 x V_{CCIO}	0.51 x V_{CCIO}	0.49 x V_{CCIO}	0.5 x V_{CCIO}	0.51 x V_{CCIO}
SSTL 135 Class I, II	1.283	1.35	1.418	0.49 x V_{CCIO}	0.5 x V_{CCIO}	0.51 x V_{CCIO}	0.49 x V_{CCIO}	0.5 x V_{CCIO}	0.51 x V_{CCIO}
SSTL 125 Class I, II	1.19	1.25	1.26	0.49 x V_{CCIO}	0.5 x V_{CCIO}	0.51 x V_{CCIO}	0.49 x V_{CCIO}	0.5 x V_{CCIO}	0.51 x V_{CCIO}
HSTL-18 Class I, II	1.71	1.8	1.89	0.85	0.9	0.95	—	V_{CCIO}/2	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.68	0.75	0.9	—	V_{CCIO}/2	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.47 x V_{CCIO}	0.5 x V_{CCIO}	0.53 x V_{CCIO}	—	V_{CCIO}/2	—
HSUL-12	1.14	1.2	1.3	0.49 x V_{CCIO}	0.5 x V_{CCIO}	0.51 x V_{CCIO}	—	—	—

Table 2–16. Single-Ended SSTL and HSTL I/O Standards Signal Specifications for Arria V Devices—*Preliminary* (Part 1 of 2)

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{oi} (mA)	I_{oh} (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL-2 Class I	–0.3	V_{REF} –0.15	V_{REF} + 0.15	V_{CCIO} + 0.3	V_{REF} – 0.31	V_{REF} + 0.31	V_{TT} – 0.608	V_{TT} + 0.608	8.1	–8.1
SSTL-2 Class II	–0.3	V_{REF} –0.15	V_{REF} + 0.15	V_{CCIO} + 0.3	V_{REF} – 0.31	V_{REF} + 0.31	V_{TT} – 0.81	V_{TT} + 0.81	16.2	–16.2
SSTL-18 Class I	–0.3	V_{REF} –0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} – 0.25	V_{REF} + 0.25	V_{TT} – 0.603	V_{TT} + 0.603	6.7	–6.7
SSTL-18 Class II	–0.3	V_{REF} –0.125	V_{REF} + 0.125	V_{CCIO} + 0.3	V_{REF} – 0.25	V_{REF} + 0.25	0.28	V_{CCIO} –0.28	13.4	–13.4
SSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.175	V_{REF} + 0.175	0.2 x V_{CCIO}	0.8 x V_{CCIO}	8	–8
SSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.175	V_{REF} + 0.175	0.2 x V_{CCIO}	0.8 x V_{CCIO}	16	–16

Table 2–16. Single-Ended SSTL and HSTL I/O Standards Signal Specifications for Arria V Devices—*Preliminary* (Part 2 of 2)

I/O Standard	$V_{IL(DC)}$ (V)		$V_{IH(DC)}$ (V)		$V_{IL(AC)}$ (V)	$V_{IH(AC)}$ (V)	V_{OL} (V)	V_{OH} (V)	I_{ol} (mA)	I_{oh} (mA)
	Min	Max	Min	Max	Max	Min	Max	Min		
SSTL 135	—	V_{REF} – 0.09	V_{REF} + 0.09	—	V_{REF} – 0.16	V_{REF} + 0.16	TBD (1)	TBD (1)	TBD (1)	TBD (1)
SSTL 125	—	V_{REF} – 0.85	V_{REF} + 0.85	—	V_{REF} – 0.15	V_{REF} + 0.15	TBD (1)	TBD (1)	TBD (1)	TBD (1)
HSTL-18 Class I	—	V_{REF} –0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	8	–8
HSTL-18 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	16	–16
HSTL-15 Class I	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} – 0.4	8	–8
HSTL-15 Class II	—	V_{REF} – 0.1	V_{REF} + 0.1	—	V_{REF} – 0.2	V_{REF} + 0.2	0.4	V_{CCIO} –0.4	16	–16
HSTL-12 Class I	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	0.25 x V_{CCIO}	0.75 x V_{CCIO}	8	–8
HSTL-12 Class II	–0.15	V_{REF} – 0.08	V_{REF} + 0.08	V_{CCIO} + 0.15	V_{REF} – 0.15	V_{REF} + 0.15	0.25 x V_{CCIO}	0.75 x V_{CCIO}	16	–16
HSUL-12	—	V_{REF} – 0.13	V_{REF} + 0.13	—	V_{REF} – 0.22	V_{REF} + 0.22	0.1 x V_{CCIO}	0.9 x V_{CCIO}	TBD (1)	TBD (1)

Note to Table 2–16:

(1) Pending silicon characterization.

Table 2–17. Differential SSTL I/O Standards for Arria V Devices—*Preliminary*

I/O Standard	V_{CCIO} (V)			$V_{SWING(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{SWING(AC)}$ (V)		$V_{OX(AC)}$ (V)		
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Max	Min	Typ	Max
SSTL-2 Class I, II	2.375	2.5	2.625	0.3	V_{CCIO} + 0.6	V_{CCIO}/2 – 0.2	—	V_{CCIO}/2 + 0.2	0.62	V_{CCIO} + 0.6	V_{CCIO}/2 – 0.15	—	V_{CCIO}/2 + 0.15
SSTL-18 Class I, II	1.71	1.8	1.89	0.25	V_{CCIO} + 0.6	V_{CCIO}/2 – 0.175	—	V_{CCIO}/2 + 0.175	0.5	V_{CCIO} + 0.6	V_{CCIO}/2 – 0.125	—	V_{CCIO}/2 + 0.125
SSTL-15 Class I, II	1.425	1.5	1.575	0.2	–0.2	–0.15	—	0.15	–0.35	0.35	—	V_{CCIO}/2	—
SSTL 135	1.283	1.35	1.45	0.2	–0.2	V_{REF} – 0.135	V_{CCIO}/2	V_{REF} + 0.135	TBD (1)	TBD (1)	V_{REF} –0.15	—	V_{REF} + 0.15
SSTL 125	1.19	1.25	1.31	TBD (1)	—	TBD (1)	V_{CCIO}/2	TBD (1)	TBD (1)	—	TBD (1)	TBD (1)	TBD (1)

Note to Table 2–17:

(1) Pending silicon characterization.

Table 2–18. Differential HSTL I/O Standards for Arria V Devices—*Preliminary*

I/O Standard	V_{CCIO} (V)			$V_{DIF(DC)}$ (V)		$V_{X(AC)}$ (V)			$V_{CM(DC)}$ (V)			$V_{DIF(AC)}$ (V)	
	Min	Typ	Max	Min	Max	Min	Typ	Max	Min	Typ	Max	Min	Max
HSTL-18 Class I, II	1.71	1.8	1.89	0.2	—	0.78	—	1.12	0.78	—	1.12	0.4	—
HSTL-15 Class I, II	1.425	1.5	1.575	0.2	—	0.68	—	0.9	0.68	—	0.9	0.4	—
HSTL-12 Class I, II	1.14	1.2	1.26	0.16	V_{CCIO} + 0.3	—	0.5 x V_{CCIO}	—	0.4 x V_{CCIO}	0.5 x V_{CCIO}	0.6 x V_{CCIO}	0.3	V_{CCIO} + 0.48
HSUL-12	1.14	1.2	1.3	0.26	0.26	0.5 x V_{CCIO} – 0.12	0.5 x V_{CCIO}	0.5 x V_{CCIO} +0.12	0.4 x V_{CCIO}	0.5 x V_{CCIO}	0.6 x V_{CCIO}	0.44	0.44

Table 2–19. Differential I/O Standard Specifications for Arria V Devices—*Preliminary* (1)

I/O Standard	V_{CCIO} (V)			V_{ID} (mV)			$V_{ICM(DC)}$ (V)		V_{OD} (V) (2)			V_{OCM} (V) (2)		
	Min	Typ	Max	Min	Condition	Max	Min	Max	Min	Typ	Max	Min	Typ	Max
PCML	(3)													
2.5 V LVDS	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.05	1.8	0.247	—	0.6	1.125	1.25	1.375
						—	1.05	1.55	0.247	—	0.6	1.125	1.25	1.375
RSDS (HIO)	2.375	2.5	2.625	100	V_{CM} = 1.25 V	—	0.3	1.4	0.1	0.2	0.6	0.5	1.2	1.4
Mini-LVDS (HIO)	2.375	2.5	2.625	200	—	600	0.4	1.325	0.25	—	0.6	1	1.2	1.4
LVPECL	2.375	2.5	2.625	300	—	—	0.6	1.8	—	—	—	—	—	—

Notes to Table 2–19:

(1) The 1.4-V and 1.5-V **PCML** transceiver I/O standard specifications are described in "Transceiver Performance Specifications" on page 2–14.

(2) RL range: $90 \leq RL \leq 110\ \Omega$.

(3) Transmitter, receiver, and input reference clock pins of high-speed transceivers use the **PCML** I/O standard. For transmitter, receiver, and reference clock I/O pin specifications, refer to Table 2–20 and Table 2–21.

Power Consumption

Altera offers two ways to estimate power consumption for a design—the Excel-based Early Power Estimator (EPE) and the Quartus® II PowerPlay Power Analyzer feature.

You typically use the interactive Excel-based EPE before designing the FPGA to get a magnitude estimate of the device power. The Quartus II PowerPlay Power Analyzer provides better quality estimates based on the specifics of the design after you complete place-and-route. The PowerPlay Power Analyzer can apply a combination of user-entered, simulation-derived, and estimated signal activities that, when combined with detailed circuit models, yields very accurate power estimates.

For more information about power estimation tools, refer to the *PowerPlay Early Power Estimator User Guide* and the *PowerPlay Power Analysis* chapter in the *Quartus II Handbook*.

Switching Characteristics

This section provides performance characteristics of Arria V core and periphery blocks for commercial grade devices.

These characteristics can be designated as Preliminary or Final.

- Preliminary characteristics are created using simulation results, process data, and other known parameters. The title of these tables show the designation as "Preliminary."
- Final numbers are based on actual silicon characterization and testing. The numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions. There are no preliminary designations on finalized tables.

Transceiver Performance Specifications

This section describes transceiver performance specifications.

Table 2–20 and Table 2–21 list the Arria V transceiver specifications.

Table 2–20. Transceiver Specifications for Arria V GX Devices—*Preliminary* (1) (Part 1 of 3)

Symbol/ Description	Conditions	–4 Commercial Speed Grade			–5 Commercial/Industrial Speed Grade			–6 Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Reference Clock											
Supported I/O Standards	**1.2 V PCML, 1.4 V PCML, 1.5 V PCML, 2.5 V PCML, Differential LVPECL** (2), **HCSL**, and **LVDS**										
Input frequency from REFCLK input pins	—	27	—	710	27	—	710	27	—	710	MHz
Duty cycle	—	45	—	55	45	—	55	45	—	55	%
Peak-to-peak differential input voltage	—	200	—	2000	200	—	2000	200	—	2000	mV
Spread-spectrum modulating clock frequency	PCI Express® (PCIe®)	30	—	33	30	—	33	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to –0.5%	—	—	0 to –0.5%	—	—	0 to –0.5%	—	—
On-chip termination resistors	—	—	100	—	—	100	—	—	100	—	Ω
V_{ICM} (AC coupled)	—		1.1 (3)			1.1 (3)			1.1 (3)		V
V_{ICM} (DC coupled)	**HCSL** I/O standard for the PCIe reference clock	250	—	550	250	—	550	250	—	550	mV
R_{REF}	—	—	2000 ±1%	—	—	2000 ±1%	—	—	2000 ±1%	—	Ω

Table 2–20. Transceiver Specifications for Arria V GX Devices—*Preliminary* (1) (Part 2 of 3)

Symbol/ Description	Conditions	–4 Commercial Speed Grade			–5 Commercial/Industrial Speed Grade			–6 Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Transceiver Clocks											
`fixedclk` clock frequency	PCIe Receiver Detect	—	125	—	—	125	—	—	125	—	MHz
Avalon®-Memory-Mapped (Avalon-MM) PHY management clock frequency	< 150										MHz
Receiver											
Supported I/O Standards	**1.5 V PCML, 2.5 V PCML, LVPECL**, and **LVDS**										
Data rate	—	611	—	6553	611	—	6553	611	—	3125	Mbps
Absolute V_{MAX} for a receiver pin (4)	—	—	—	1.2	—	—	1.2	—	—	1.2	V
Absolute V_{MIN} for a receiver pin	—	–0.4	—	—	–0.4	—	—	–0.4	—	—	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) before device configuration	—	—	—	1.6	—	—	1.6	—	—	1.6	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) after device configuration	—	—	—	2.2	—	—	2.2	—	—	2.2	V
Minimum differential eye opening at the receiver serial input pins (5)	—	85	—	—	85	—	—	85	—	—	mV
Differential on-chip termination resistors	85-Ω setting	—	85	—	—	85	—	—	85	—	Ω
	100-Ω setting	—	100	—	—	100	—	—	100	—	Ω
	120-Ω setting	—	120	—	—	120	—	—	120	—	Ω
	150-Ω setting	—	150	—	—	150	—	—	150	—	Ω
Differential and common mode return loss	PCIe (Gen1 and Gen2), GIGE, XAUI, SDI, CPRI, OBSAI	Compliant									—
Programmable ppm detector (6)	—	±62.5, 100, 125, 200, 250, 300, 500, and 1000									ppm
Run Length	—	—	—	200	—	—	200	—	—	200	UI
Programmable equalization	—	—	—	4	—	—	4	—	—	4	dB

Table 2–20. Transceiver Specifications for Arria V GX Devices—*Preliminary* (1) (Part 3 of 3)

Symbol/ Description	Conditions	–4 Commercial Speed Grade			–5 Commercial/Industrial Speed Grade			–6 Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Programmable DC gain	DC Gain Setting = 0	—	0	—	—	0	—	—	0	—	dB
	DC Gain Setting = 1	—	3	—	—	3	—	—	3	—	dB
Transmitter											
Supported I/O Standards	**1.5 V PCML**										
Data rate	—	611	—	6553	611	—	6553	611	—	3125	Mbps
V_{OCM}	—	—	650	—	—	650	—	—	650	—	mV
Differential on-chip termination resistors	85-Ω setting	—	85	—	—	85	—	—	85	—	Ω
	100-Ω setting	—	100	—	—	100	—	—	100	—	Ω
	120-Ω setting	—	120	—	—	120	—	—	120	—	Ω
	150-Ω setting	—	150	—	—	150	—	—	150	—	Ω
Rise time (7)	—	30	—	160	30	—	160	30	—	160	ps
Fall time (7)	—	30	—	160	30	—	160	30	—	160	ps
CMU PLL											
Supported data range	—	611	—	6553	611	—	6553	611	—	3125	Mbps
Transceiver-FPGA Fabric Interface											
Interface speed (single-width mode)	—	25	—	156.25	25	—	156.25	25	—	156.25	MHz
Interface speed (double-width mode)	—	25	—	159.375	25	—	159.375	25	—	159.375	MHz

Notes to Table 2–20:

(1) Speed grades shown in Table 2–20 refer to the Transceiver Speed Grade in the device ordering code. For more information about device ordering codes, refer to the *Overview for Arria V Device Family* chapter.

(2) Differential LVPECL signal levels must comply to the minimum and maximum peak-to-peak differential input voltage specified in this table.

(3) The reference clock common mode voltage is equal to the V_{CCR_GXB} power supply level.

(4) The device cannot tolerate prolonged operation at this absolute maximum.

(5) The differential eye opening specification at the receiver input pins assumes that you have disabled the **Receiver Equalization** feature. If you enable the **Receiver Equalization** feature, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

(6) The rate match FIFO supports only up to ±300 parts per million (ppm).

(7) The Quartus II software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.

Table 2–21. Transceiver Specifications for Arria V GT Devices—*Preliminary* (1) (Part 1 of 2)

Symbol/ Description	Conditions	–5 Industrial Speed Grade			Unit
		Min	Typ	Max	
Reference Clock					
Supported I/O Standards	**1.2 V PCML**, **1.4 V PCML**, **1.5 V PCML**, **2.5 V PCML**, **Differential LVPECL** (2), **HCSL**, and **LVDS**				
Input frequency from REFCLK input pins	—	27	—	710	MHz
Duty cycle	—	45	—	55	%
Peak-to-peak differential input voltage	—	200	—	2000	mV
Spread-spectrum modulating clock frequency	PCI Express® (PCIe®)	30	—	33	kHz
Spread-spectrum downspread	PCIe	—	0 to –0.5%	—	—
On-chip termination resistors	—	—	100	—	Ω
V_{ICM} (AC coupled)	—		1.1 (3)		V
V_{ICM} (DC coupled)	**HCSL** I/O standard for the PCIe reference clock	250	—	550	mV
R_{REF}	—	—	2000 ±1%	—	Ω
Transceiver Clocks					
fixedclk clock frequency	PCIe Receiver Detect	—	125	—	MHz
Avalon-MM PHY management clock frequency	< 150				MHz
Receiver					
Supported I/O Standards	**1.5 V PCML**, **2.5 V PCML**, **LVPECL**, and **LVDS**				
Data rate (6-Gbps Transceiver)	—	611	—	6375	Mbps
Data rate (10-Gbps transceiver)	—	6.376	9.8304	10.3125	Gbps
Absolute V_{MAX} for a receiver pin (4)	—	—	—	1.2	V
Absolute V_{MIN} for a receiver pin	—	–0.4	—	—	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) before device configuration	—	—	—	1.6	V
Maximum peak-to-peak differential input voltage V_{ID} (diff p-p) after device configuration	—	—	—	2.2	V
Minimum differential eye opening at the receiver serial input pins (5)	—	85	—	—	mV
Differential on-chip termination resistors	85-Ω setting		85		Ω
	100-Ω setting		100		Ω
	120-Ω setting		120		Ω
	150-Ω setting		150		Ω

Table 2–21. Transceiver Specifications for Arria V GT Devices—*Preliminary* (1) (Part 2 of 2)

Symbol/ Description	Conditions	–5 Industrial Speed Grade			Unit
		Min	Typ	Max	
Differential and common mode return loss	PCIe (Gen1 and Gen2), GIGE, XAUI, SDI, CPRI, OBSAI, SFI	Compliant			—
Programmable ppm detector (6)	—	±62.5, 100, 125, 200, 250, 300, 500, and 1000			ppm
Run Length	—	—	—	200	UI
Programmable equalization	—	—	—	4	dB
Programmable DC gain	DC Gain Setting = 0	—	0	—	dB
	DC Gain Setting = 1	—	3	—	dB
Transmitter					
Supported I/O Standards	**1.5 V PCML**				
Data rate (6-Gbps transceiver)	—	611	—	6375	Mbps
Data rate (10-Gbps transceiver)	—	6.376	9.8304	10.3125	Gbps
V_{OCM}	—	—	650	—	mV
Differential on-chip termination resistors	85-Ω setting	—	85	—	Ω
	100-Ω setting	—	100	—	Ω
	120-Ω setting	—	120	—	Ω
	150-Ω setting	—	150	—	Ω
Rise time (7)	—	30	—	160	ps
Fall time (7)	—	30	—	160	ps
CMU PLL					
Supported data range	—	0.611	—	10.3125	Gbps
Transceiver-FPGA Fabric Interface					
Interface speed (80-bit mode)	—	25	—	159.375	MHz
Interface speed (single-width mode)	—	25	—	156.25	MHz
Interface speed (double-width mode)	—	25	—	159.375	MHz

Notes to Table 2–21:

(1) Speed grades shown in Table 2–21 refer to the Transceiver Speed Grade in the device ordering code. For more information about device ordering codes, refer to the *Overview for Arria V Device Family* chapter.

(2) Differential **LVPECL** signal levels must comply to the minimum and maximum peak-to-peak differential input voltage specified in this table.

(3) The reference clock common mode voltage is equal to the V_{CCR_GXB} power supply level.

(4) The device cannot tolerate prolonged operation at this absolute maximum.

(5) The differential eye opening specification at the receiver input pins assumes that you have disabled the **Receiver Equalization** feature. If you enable the **Receiver Equalization** feature, the receiver circuitry can tolerate a lower minimum eye opening, depending on the equalization level.

(6) The rate match FIFO supports only up to ±300 ppm.

(7) The Quartus II software automatically selects the appropriate slew rate depending on the configured data rate or functional mode.

Table 2–22 and Table 2–23 list the transceiver block jitter specification for Arria V devices.

Table 2–22. Transceiver Block Jitter Specification for Arria V GX Devices—*Preliminary* (Part 1 of 4)

Symbol/ Description	Conditions	–4 Commercial Speed Grade			–5 Commercial/ Industrial Speed Grade			–6 Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
CPRI Transmit Jitter Generation (1)											
Total Jitter	E.6.HV, E.12.HV Pattern = CJPAT	—	—	0.279	—	—	0.279	—	—	0.279	UI
	E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJTPAT	—	—	0.35	—	—	0.35	—	—	0.35	UI
Deterministic Jitter	E.6.HV, E.12.HV Pattern = CJPAT	—	—	0.14	—	—	0.14	—	—	0.14	UI
	E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJTPAT	—	—	0.17	—	—	0.17	—	—	0.17	UI
CPRI Receiver Jitter Tolerance (1)											
Total jitter tolerance	E.6.HV, E.12.HV Pattern = CJPAT	> 0.66			> 0.66			> 0.66			UI
Deterministic jitter tolerance	E.6.HV, E.12.HV Pattern = CJPAT	> 0.4			> 0.4			> 0.4			UI
Total jitter tolerance	E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJTPAT	> 0.65			> 0.65			> 0.65			UI
Deterministic jitter tolerance	E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJTPAT	> 0.37			> 0.37			> 0.37			UI
Combined deterministic and random jitter tolerance	E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJTPAT	> 0.55			> 0.55			> 0.55			UI
OBSAI Transmit Jitter Generation (2)											
Total jitter at 768 Mbps, 1536 Mbps, and 3072 Mbps	REFCLK = 153.6 MHz Pattern = CJPAT	—	—	0.35	—	—	0.35	—	—	0.35	UI
Deterministic jitter at 768 Mbps, 1536 Mbps, and 3072 Mbps	REFCLK = 153.6 MHz Pattern = CJPAT	—	—	0.17	—	—	0.17	—	—	0.17	UI

Table 2–22. Transceiver Block Jitter Specification for Arria V GX Devices—*Preliminary* (Part 2 of 4)

Symbol/ Description	Conditions	–4 Commercial Speed Grade			–5 Commercial/ Industrial Speed Grade			–6 Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
OBSAI Receiver Jitter Tolerance (2)											
Deterministic jitter tolerance at 768 Mbps, 1536 Mbps, and 3072 Mbps	Pattern = CJPAT		> 0.37			> 0.37			> 0.37		UI
Combined deterministic and random jitter tolerance at 768 Mbps, 1536 Mbps, and 3072 Mbps	Pattern = CJPAT		> 0.55			> 0.55			> 0.55		UI
Sinusoidal Jitter tolerance at 768 Mbps	Jitter Frequency = 5.4 KHz Pattern = CJPAT		> 8.5			> 8.5			> 8.5		UI
	Jitter Frequency = 460 MHz to 20 MHz Pattern = CJPAT		> 0.1			> 0.1			> 0.1		UI
Sinusoidal Jitter tolerance at 1536 Mbps	Jitter Frequency = 10.9 KHz Pattern = CJPAT		> 8.5			> 8.5			> 8.5		UI
	Jitter Frequency = 921.6 MHz to 20 MHz Pattern = CJPAT		> 0.1			> 0.1			> 0.1		UI
Sinusoidal Jitter tolerance at 3072 Mbps	Jitter Frequency = 21.8 KHz Pattern = CJPAT		> 8.5			> 8.5			> 8.5		UI
	Jitter Frequency = 1843.2 MHz to 20 MHz Pattern = CJPAT		> 0.1			> 0.1			> 0.1		UI
Serial RapidIO® (SRIO) Transmit Jitter Generation (3)											
Deterministic jitter (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	—	—	0.17	—	—	0.17	—	—	0.17	UI
Total jitter (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	—	—	0.35	—	—	0.35	—	—	0.35	UI

Table 2–22. Transceiver Block Jitter Specification for Arria V GX Devices—*Preliminary* (Part 3 of 4)

Symbol/ Description	Conditions	–4 Commercial Speed Grade			–5 Commercial/ Industrial Speed Grade			–6 Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
SRIO Receiver Jitter Tolerance (3)											
Deterministic jitter tolerance (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	> 0.37			> 0.37			> 0.37			UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	> 0.55			> 0.55			> 0.55			UI
Sinusoidal jitter tolerance (peak-to-peak)	Jitter Frequency = 22.1 KHz Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	> 8.5			> 8.5			> 8.5			UI
	Jitter Frequency = 1.875 MHz Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	> 0.1			> 0.1			> 0.1			UI
	Jitter Frequency = 20 MHz Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	> 0.1			> 0.1			> 0.1			UI
GIGE Transmit Jitter Generation (4)											
Deterministic jitter (peak-to-peak)	Pattern = CRPAT	—	—	0.14	—	—	0.14	—	—	0.14	UI
Total jitter (peak-to-peak)	Pattern = CRPAT	—	—	0.279	—	—	0.279	—	—	0.279	UI
GIGE Receiver Jitter Tolerance (4)											
Deterministic jitter tolerance (peak-to-peak)	Pattern = CJPAT	> 0.4			> 0.4			> 0.4			UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Pattern = CJPAT	> 0.66			> 0.66			> 0.66			UI

Table 2–22. Transceiver Block Jitter Specification for Arria V GX Devices—*Preliminary* (Part 4 of 4)

Symbol/ Description	Conditions	–4 Commercial Speed Grade			–5 Commercial/ Industrial Speed Grade			–6 Commercial Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
HiGig Transmit Jitter Generation (5)											
Deterministic jitter (peak-to-peak)	Data Rate = 3.75 Gbps Pattern = CJPAT	—	—	0.17	—	—	—	—	—	—	UI
Total jitter (peak-to-peak)	Data Rate = 3.75 Gbps Pattern = CJPAT	—	—	0.35	—	—	—	—	—	—	UI

Notes to Table 2–22:

(1) The jitter numbers for CPRI are compliant to the CPRI Specification V3.0.
(2) The jitter numbers for OBSAI are compliant to the OBSAI RP3 Specification V4.1.
(3) The jitter numbers for SRIO are compliant to the RapidIO Specification 1.3.
(4) The jitter numbers for GIGE are compliant to the IEEE802.3-2002 Specification.
(5) The jitter numbers for HiGig are compliant to the IEEE802.3ae-2002 Specification.

Table 2–23. Transceiver Block Jitter Specification for Arria V GT Devices—*Preliminary* (Part 1 of 4)

Symbol/ Description	Conditions	–5 Industrial Speed Grade			Unit
		Min	Typ	Max	
SFI Transmit Jitter Generation (1)					
Deterministic Jitter	Data Rate = 9.8304, 10.3125 Gbps	—	—	0.1	UI
Total Jitter	Pattern = PRBS31	—	—	0.28	UI
SFI Receive Jitter Tolerance (1)					
99% Jitter Tolerance	Data Rate = 9.8304, 10.3125 Gbps	>0.42			UI
Total Jitter	Pattern = PRBS31	>0.70			UI
CPRI Transmit Jitter Generation (2)					
Total Jitter	E.6.HV, E.12.HV Pattern = CJPAT	—	—	0.279	—
	E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJTPAT	—	—	0.35	—
Deterministic Jitter	E.6.HV, E.12.HV Pattern = CJPAT	—	—	0.14	—
	E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJTPAT	—	—	0.17	—

Table 2–23. Transceiver Block Jitter Specification for Arria V GT Devices—*Preliminary* (Part 2 of 4)

Symbol/ Description	Conditions	–5 Industrial Speed Grade			Unit
		Min	Typ	Max	
CPRI Receive Jitter Generation (2)					
Total jitter tolerance	E.6.HV, E.12.HV Pattern = CJPAT		> 0.66		> 0.66
Deterministic jitter tolerance	E.6.HV, E.12.HV Pattern = CJPAT		> 0.4		> 0.4
Total jitter tolerance	E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJTPAT		> 0.65		> 0.65
Deterministic jitter tolerance	E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJTPAT		> 0.37		> 0.37
Combined deterministic and random jitter tolerance	E.6.LV, E.12.LV, E.24.LV, E.30.LV Pattern = CJTPAT		> 0.55		> 0.55
OBSAI Transmit Jitter Generation (3)					
Total jitter at 768 Mbps, 1536 Mbps, and 3072 Mbps	REFCLK = 153.6MHz Pattern = CJPAT	—	—	0.35	—
Deterministic jitter at 768 Mbps, 1536 Mbps, and 3072 Mbps	REFCLK = 153.6MHz Pattern = CJPAT	—	—	0.17	—
OBSAI Receiver Jitter Tolerance (3)					
Deterministic jitter tolerance at 768 Mbps, 1536 Mbps, and 3072 Mbps	Pattern = CJPAT		> 0.37		> 0.37
Combined deterministic and random jitter tolerance at 768 Mbps, 1536 Mbps, and 3072 Mbps	Pattern = CJPAT		> 0.55		> 0.55
Sinusoidal Jitter tolerance at 768 Mbps	Jitter Frequency = 5.4 KHz Pattern = CJPAT		> 8.5		> 8.5
	Jitter Frequency = 460 MHz to 20 MHz Pattern = CJPAT		> 0.1		> 0.1
Sinusoidal Jitter tolerance at 1536 Mbps	Jitter Frequency = 10.9 KHz Pattern = CJPAT		> 8.5		> 8.5
	Jitter Frequency = 921.6 MHz to 20 MHz Pattern = CJPAT		> 0.1		> 0.1

Table 2–23. Transceiver Block Jitter Specification for Arria V GT Devices—*Preliminary* (Part 3 of 4)

Symbol/ Description	Conditions	–5 Industrial Speed Grade			Unit
		Min	Typ	Max	
Sinusoidal Jitter tolerance at 3072 Mbps	Jitter Frequency = 21.8 KHz Pattern = CJPAT		> 8.5		> 8.5
	Jitter Frequency = 1843.2 MHz to 20 MHz Pattern = CJPAT		> 0.1		> 0.1
SRIO Transmit Jitter Generation (4)					
Deterministic jitter (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	—	—	0.17	UI
Total jitter (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT	—	—	0.35	UI
SRIO Receiver Jitter Tolerance (4)					
Deterministic jitter tolerance (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT		> 0.37		UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT		> 0.55		UI
Sinusoidal jitter tolerance (peak-to-peak)	Jitter Frequency = 22.1 KHz Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT		> 8.5		UI
	Jitter Frequency = 1.875 MHz Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT		> 0.1		UI
	Jitter Frequency = 20 MHz Data Rate = 1.25, 2.5, 3.125 Gbps Pattern = CJPAT		> 0.1		UI
GIGE Transmit Jitter Generation (5)					
Deterministic jitter (peak-to-peak)	Pattern = CRPAT	—	—	0.14	UI
Total jitter (peak-to-peak)	Pattern = CRPAT	—	—	0.279	UI
GIGE Receiver Jitter Tolerance (5)					
Deterministic jitter tolerance (peak-to-peak)	Pattern = CJPAT		> 0.4		UI
Combined deterministic and random jitter tolerance (peak-to-peak)	Pattern = CJPAT		> 0.66		UI

Table 2–23. Transceiver Block Jitter Specification for Arria V GT Devices—*Preliminary* (Part 4 of 4)

Symbol/ Description	Conditions	–5 Industrial Speed Grade			Unit
		Min	Typ	Max	
HiGig Transmit Jitter Generation (6)					
Deterministic jitter (peak-to-peak)	Data Rate = 3.75 Gbps Pattern = CJPAT	—	—	0.17	UI
Total jitter (peak-to-peak)	Data Rate = 3.75 Gbps Pattern = CJPAT	—	—	0.35	UI

Notes to Table 2–23:

(1) The jitter numbers for SFI are compliant to SFF-8431 Specification.
(2) The jitter numbers for CPRI are compliant to the CPRI Specification V3.0.
(3) The jitter numbers for OBSAI are compliant to the OBSAI RP3 Specification V4.1.
(4) The jitter numbers for SRIO are compliant to the RapidIO Specification 1.3.
(5) The jitter numbers for GIGE are compliant to the IEEE802.3-2002 Specification.
(6) The jitter numbers for HiGig are compliant to the IEEE802.3ae-2002 Specification.

Core Performance Specifications

This section describes the clock tree, phase-locked loop (PLL), digital signal processing (DSP), memory blocks and temperature sensing diode specifications.

Clock Tree Specifications

Table 2–24 lists the clock tree specifications for Arria V devices.

Table 2–24. Clock Tree Performance for Arria V Devices—*Preliminary*

Performance				Unit
Symbol	–C4 Speed Grade	–C5, I5 Speed Grade	–C6 Speed Grade	
Global clock and Regional clock	625	625	525	MHz
Peripheral clock	450	400	350	MHz

PLL Specifications

Table 2–25 lists the Arria V PLL specifications when operating in both the commercial junction temperature range (0° to 85°C) and the industrial junction temperature range (–40° to 100°C).

Table 2–25. PLL Specifications for Arria V Devices—*Preliminary* (1) (Part 1 of 3)

Symbol	Parameter	Min	Typ	Max	Unit
f_{IN}	Input clock frequency (–4 speed grade)	5	—	670 (2)	MHz
	Input clock frequency (–5 speed grade)	5	—	622 (2)	MHz
	Input clock frequency (–6 speed grade)	5	—	500 (2)	MHz
f_{INPFD}	Integer input clock frequency to the PFD	5	—	325	MHz
f_{FINPFD}	Fractional input clock frequency to the PFD	50	—	TBD (1)	MHz

Table 2–25. PLL Specifications for Arria V Devices—*Preliminary* (1) (Part 2 of 3)

Symbol	Parameter	Min	Typ	Max	Unit
f_{VCO}	PLL VCO operating range (–4 speed grade)	600	—	1600	MHz
	PLL VCO operating range (–5 speed grade)	600	—	1400	MHz
	PLL VCO operating range (–6 speed grade)	600	—	1300	MHz
$t_{EINDUTY}$	Input clock or external feedback clock input duty cycle	40	—	60	%
f_{OUT}	Output frequency for internal global or regional clock (–4 speed grade)	—	—	500 (3)	MHz
	Output frequency for internal global or regional clock (–5 speed grade)	—	—	500 (3)	MHz
	Output frequency for internal global or regional clock (–6 speed grade)	—	—	400 (3)	MHz
f_{OUT_EXT}	Output frequency for external clock output (–4 speed grade)	—	—	670 (3)	MHz
	Output frequency for external clock output (–5 speed grade)	—	—	622 (3)	MHz
	Output frequency for external clock output (–6 speed grade)	—	—	500 (3)	MHz
$t_{OUTDUTY}$	Duty cycle for external clock output (when set to 50%)	45	50	55	%
t_{FCOMP}	External feedback clock compensation time	—	—	10	ns
$t_{CONFIGPHASE}$	Time required to reconfigure phase shift	—	—	TBD (1)	—
$t_{DYCONFIGCLK}$	Dynamic Configuration Clock	—	—	100	MHz
t_{LOCK}	Time required to lock from end-of-device configuration or deassertion of `areset`	—	—	1	ms
t_{DLOCK}	Time required to lock dynamically (after switchover or reconfiguring any non-post-scale counters/delays)	—	—	1	ms
f_{CLBW}	PLL closed-loop low bandwidth	—	0.3	—	MHz
	PLL closed-loop medium bandwidth	—	1.5	—	MHz
	PLL closed-loop high bandwidth (8)	—	4	—	MHz
t_{PLL_PSERR}	Accuracy of PLL phase shift	—	—	±50	ps
t_{ARESET}	Minimum pulse width on the `areset` signal	10	—	—	ns
t_{INCCJ} (4), (5)	Input clock cycle-to-cycle jitter ($F_{REF} \geq 100$ MHz)	—	—	0.15	UI (p-p)
	Input clock cycle-to-cycle jitter ($F_{REF} < 100$ MHz)	—	—	+750	ps (p-p)
t_{OUTPJ_DC} (6)	Period jitter for dedicated clock output ($F_{OUT} \geq 100$ MHz)	—	—	TBD (1)	ps (p-p)
	Period jitter for dedicated clock output ($F_{OUT} < 100$ MHz)	—	—	TBD (1)	mUI (p-p)
t_{OUTCCJ_DC} (6)	Cycle-to-cycle jitter for dedicated clock output ($F_{OUT} \geq 100$ MHz)	—	—	TBD (1)	ps (p-p)
	Cycle-to-cycle jitter for dedicated clock output ($F_{OUT} < 100$ MHz)	—	—	TBD (1)	mUI (p-p)
t_{OUTPJ_IO} (6), (9)	Period Jitter for clock output on the regular I/O ($F_{OUT} \geq 100$ MHz)	—	—	TBD (1)	ps (p-p)
	Period Jitter for clock output on the regular I/O ($F_{OUT} < 100$ MHz)	—	—	TBD (1)	mUI (p-p)
t_{OUTCCJ_IO} (6), (9)	Cycle-to-cycle jitter for clock output on the regular I/O ($F_{OUT} \geq 100$ MHz)	—	—	TBD (1)	ps (p-p)
	Cycle-to-cycle jitter for clock output on the regular I/O ($F_{OUT} < 100$ MHz)	—	—	TBD (1)	mUI (p-p)

Table 2–25. PLL Specifications for Arria V Devices—*Preliminary* (1) (Part 3 of 3)

Symbol	Parameter	Min	Typ	Max	Unit
$t_{OUTPJ\_DC\_F}$	Period jitter for dedicated clock output in fractional mode	—	—	TBD (1)	—
$t_{OUTCCJ\_DC\_F}$	Cycle-to-cycle jitter for dedicated clock output in fractional mode	—	—	TBD (1)	—
$t_{OUTPJ\_IO\_F}$	Period Jitter for clock output on the regular I/O in fractional mode	—	—	TBD (1)	—
$t_{OUTCCJ\_IO\_F}$	Cycle-to-cycle jitter for clock output on the regular I/O in fractional mode	—	—	TBD (1)	—
$t_{CASC\_OUTPJ\_DC}$ (6), (7)	Period jitter for dedicated clock output in cascaded PLLs ($F_{OUT} \geq 100$ MHz)	—	—	TBD (1)	ps (p-p)
	Period jitter for dedicated clock output in cascaded PLLs ($F_{OUT} < 100$ MHz)	—	—	TBD (1)	mUI (p-p)
t_{DRIFT}	Frequency drift after PFDENA is disabled for a duration of 100 µs	—	—	±10	%
dK_{BIT}	Bit number of Delta Sigma Modulator (DSM)	—	24	—	bits
k_{VALUE}	Numerator of Fraction	TBD (1)	8388608	TBD (1)	—
f_{RES}	Resolution of VCO frequency (f_{INPFD} =100 MHz)	—	5.96	—	Hz

Notes to Table 2–25:

(1) Pending silicon characterization.

(2) This specification is limited in the Quartus II software by the I/O maximum frequency. The maximum I/O frequency is different for each I/O standard.

(3) This specification is limited by the lower of the two: I/O f_{MAX} or F_{OUT} of the PLL.

(4) A high input jitter directly affects the PLL output jitter. To have low PLL output clock jitter, you must provide a clean clock source < 120 ps.

(5) F_{REF} is fIN/N when N = 1.

(6) Peak-to-peak jitter with a probability level of 10^{-12} (14 sigma, 99.99999999974404 % confidence level). The output jitter specification applies to the intrinsic jitter of the PLL, when an input jitter of 30 ps is applied. The external memory interface clock output jitter specifications use a different measurement method and are available in Table 2–33 on page 2–34.

(7) The cascaded PLL specification is only applicable with the following conditions:
a. Upstream PLL: 0.59 MHz ≤ Upstream PLL BW < 1 MHz
b. Downstream PLL: Downstream PLL BW > 2 MHz

(8) High bandwidth PLL settings are not supported in external feedback mode.

(9) External memory interface clock output jitter specifications use a different measurement method, which are available in Table 2–33 on page 2–34.

DSP Block Specifications

Table 2–26 lists the Arria V DSP block performance specifications.

Table 2–26. DSP Block Performance Specifications for Arria V Devices—*Preliminary*

Mode	Performance			Unit
	–C4 Speed Grade	–C5, I5 Speed Grade	–C6 Speed Grade	
Modes using One DSP Block				
Independent 9 x 9 Multiplication	370	310	220	MHz
Independent 18 x 19 Multiplication	370	310	220	MHz
Independent 18 x 18 Multiplication	370	310	220	MHz
Independent 27 x 27 Multiplication	310	250	200	MHz
Independent 18 x 25 Multiplication	370	310	220	MHz
Independent 20 x 24 Multiplication	370	310	220	MHz
Two 18 x 19 Multiplier Adder Mode	370	310	220	MHz
18 x 18 Multiplier Added Summed with 36-bit Input	370	310	220	MHz
Modes using Two DSP Blocks				
Complex 18 x 19 multiplication	370	310	220	MHz
Two 27 x 27 Multiplier Adder	310	250	200	MHz
Four 18 x 19 Multiplier Adder	370	310	220	MHz

Memory Block Specifications

Table 2–27 lists the Arria V memory block specifications.

Table 2–27. Memory Block Performance Specifications for Arria V Devices—*Preliminary*[1], [2] (Part 1 of 2)

Memory	Mode	Resources Used		Performance			Unit
		ALUTs	Memory	C4 Speed Grade	C5,I5 Speed Grade	C6 Speed Grade	
MLAB	Single port, all supported widths	0	1	500	450	400	MHz
	Simple dual-port, all supported widths	0	1	500	450	400	MHz
	Simple dual-port with read and write at the same address	0	1	400	350	300	MHz
	ROM, all supported width	—	—	500	450	400	MHz

Table 2–27. Memory Block Performance Specifications for Arria V Devices—*Preliminary*[(1), (2)] (Part 2 of 2)

Memory	Mode	Resources Used		Performance			Unit
		ALUTs	Memory	C4 Speed Grade	C5,I5 Speed Grade	C6 Speed Grade	
M10K Block	Single-port, all supported widths	0	1	400	350	285	MHz
	Simple dual-port, all supported widths	0	1	400	350	285	MHz
	Simple dual-port with the read-during-write option set to **Old Data**, all supported widths	0	1	315	275	240	MHz
	True dual port, all supported widths	0	1	400	350	285	MHz
	ROM, all supported widths	0	1	400	350	285	MHz
	Min Pulse Width (clock high time)	—	—	1,275	1,360	1,445	ps
	Min Pulse Width (clock low time)	—	—	850	1,060	1,175	ps

Notes to Table 2–27:

(1) To achieve the maximum memory block performance, use a memory block clock that comes through global clock routing from an on-chip PLL set to **50%** output duty cycle. Use the Quartus II software to report timing for this and other memory block clocking schemes.

(2) When you use the error detection cyclical redundancy check (CRC) feature, there is no degradation in f_{MAX}.

Temperature Sensing Diode Specifications

Table 2–28 lists the specifications for the Arria V internal temperature sensing diode.

Table 2–28. Internal Temperature Sensing Diode Specifications for Arria V Devices—*Preliminary*

Temperature Range	Accuracy	Offset Calibrated Option	Sampling Rate	Conversion Time	Resolution	Minimun Resolution with no Missing Codes
–40 to 100°C	±8°C	No	Frequency: 1 MHz	< 100 ms	8 bits	8 bits

Periphery Performance

This section describes periphery performance and the high-speed I/O and external memory interface.

I/O performance supports several system interfaces, such as the LVDS high-speed I/O interface, external memory interface, and the PCI/PCI-X bus interface. GPIO standards such as 3.3-, 2.5-, 1.8-, and 1.5-V **LVTTL/LVCMOS** are capable of a typical 167 MHz and 1.2 **LVCMOS** at 100 MHz interfacing frequency with a 10 pF load.

Actual achievable frequency depends on design- and system-specific factors. You must perform HSPICE/IBIS simulations based on your specific design and system setup to determine the maximum achievable frequency in your system.

High-Speed I/O Specification

Table 2–29 lists high-speed I/O timing for Arria V devices.

Table 2–29. High-Speed I/O Specifications for Arria V Devices—*Preliminary*(1), (2), (3) (Part 1 of 3)

Symbol	Conditions	–4 Speed Grade			–5 Speed Grade			–6 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
f_{HSCLK_in} (input clock frequency) True Differential I/O Standards	Clock boost factor W = 1 to 40 (5)	5	—	625	5	—	625	5	—	TBD	MHz
f_{HSCLK_in} (input clock frequency) Single Ended I/O Standards (4)	Clock boost factor W = 1 to 40 (5)	5	—	625	5	—	625	5	—	TBD	MHz
f_{HSCLK_in} (input clock frequency) Single Ended I/O Standards (3)	Clock boost factor W = 1 to 40 (5)	5	—	TBD	5	—	TBD	5	—	TBD	MHz
f_{HSCLK_OUT} (output clock frequency)	—	5	—	625 (6)	5	—	625 (6)	5	—	TBD (6)	MHz
Transmitter											
True Differential I/O Standards - f_{HSDR} (data rate)	SERDES factor J = 3 to 10	(7)	—	1250	(7)	—	1250	(7)	—	1050	Mbps
	SERDES factor J = 1 to 2, Uses DDR Registers	(7)	—	(7)	(7)	—	(7)	(7)	—	(7)	Mbps
Emulated Differential I/O Standards with Three External Output Resistor Networks - f_{HSDR} (data rate) (8)	SERDES factor J = 4 to 10	(7)	—	TBD	(7)	—	TBD	(7)	—	TBD	Mbps
$t_{x\ Jitter}$ - True Differential I/O Standards	Total Jitter for Data Rate, 600 Mbps - 1.25 Gbps	—	—	160	—	—	160	—	—	160	ps
	Total Jitter for Data Rate, < 600 Mbps	—	—	0.1	—	—	0.1	—	—	0.1	UI

Table 2–29. High-Speed I/O Specifications for Arria V Devices—*Preliminary*(1), (2), (3) (Part 2 of 3)

Symbol	Conditions	–4 Speed Grade			–5 Speed Grade			–6 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
$t_{x\ Jitter}$ - Emulated Differential I/O Standards with Three External Output Resistor Network	Total Jitter for Data Rate, 600 Mbps – 1.25 Gbps	—	—	TBD	—	—	TBD	—	—	TBD	ps
	Total Jitter for Data Rate < 600 Mbps	—	—	TBD	—	—	TBD	—	—	TBD	UI
t_{DUTY}	TX output clock duty cycle for both True and Emulated Differential I/O Standards	45	50	55	45	50	55	45	50	55	%
t_{RISE} & t_{FALL}	True Differential I/O Standards	—	—	200	—	—	200	—	—	200	ps
	Emulated Differential I/O Standards with Three External Output Resistor Networks	—	—	250	—	—	250	—	—	300	ps
TCCS	True Differential I/O Standards	—	—	150	—	—	150	—	—	150	ps
	Emulated Differential I/O Standards	—	—	300	—	—	300	—	—	300	ps
Receiver											
True Differential I/O Standards - $f_{HSDRDPA}$ (data rate)	SERDES factor J = 3 to 10	—	—	1250	—	—	1250	—	—	1050	Mbps
f_{HSDR} (data rate)	SERDES factor J = 3 to 10	(7)	—	(9)	(7)	—	(9)	(7)	—	(9)	Mbps
	SERDES factor J = 1 to 2, Uses DDR Registers	(7)	—	(7)	(7)	—	(7)	(7)	—	(7)	Mbps
DPA Mode											
DPA run length	—	—	—	10000	—	—	10000	—	—	10000	UI
Soft CDR mode											
Soft-CDR ppm tolerance	—	—	—	300	—	—	300	—	—	300	± ppm

Table 2–29. High-Speed I/O Specifications for Arria V Devices—*Preliminary* (1), (2), (3) (Part 3 of 3)

Symbol	Conditions	–4 Speed Grade			–5 Speed Grade			–6 Speed Grade			Unit
		Min	Typ	Max	Min	Typ	Max	Min	Typ	Max	
Non DPA Mode											
Sampling Window	—	—	—	300	—	—	300	—	—	300	ps

Notes to Table 2–29:

(1) When J = 3 to 10, use the serializer/deserializer (SERDES) block.
(2) When J = 1 or 2, bypass the SERDES block.
(3) This applies to LVDS source synchronous mode only.
(4) This applies to DPA and soft-CDR modes only.
(5) Clock Boost Factor (W) is the ratio between the input data rate and the input clock rate.
(6) This is achieved by using the LVDS clock network.
(7) The minimum specification depends on the clock source (for example, the PLL and clock pin) and the clock routing resource (global, regional, or local) that you use. The I/O differential buffer and input register do not have a minimum toggle rate.
(8) You must calculate the leftover timing margin in the receiver by performing link timing closure analysis. You must consider the board skew margin, transmitter channel-to-channel skew, and receiver sampling margin to determine the leftover timing margin.
(9) You can estimate the achievable maximum data rate for non-DPA mode by performing link timing closure analysis. You must consider the board skew margin, transmitter delay margin, and receiver sampling margin to determine the maximum data rate supported.

Figure 2–1 shows the DPA lock time specifications with the DPA PLL calibration option enabled.

Figure 2–1. DPA Lock Time Specification with DPA PLL Calibration Enabled

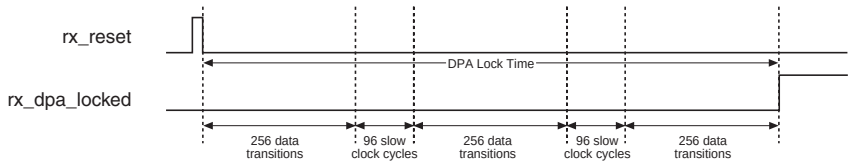


Table 2–30 lists the DPA lock time specifications for Arria V devices.

Table 2–30. DPA Lock Time Specifications for Arria V Devices—*Preliminary* (1), (2), (3)

Standard	Training Pattern	Number of Data Transitions in One Repetition of the Training Pattern	Number of Repetitions per 256 Data Transitions (4)	Maximum
SPI-4	00000000001111111111	2	128	640 data transitions
Parallel Rapid I/O	00001111	2	128	640 data transitions
	10010000	4	64	640 data transitions
Miscellaneous	10101010	8	32	640 data transitions
	01010101	8	32	640 data transitions

Notes to Table 2–30:

(1) The DPA lock time is for one channel.
(2) One data transition is defined as a 0-to-1 or 1-to-0 transition.
(3) The DPA lock time stated in this table applies to both commercial and industrial grades.
(4) This is the number of repetitions for the stated training pattern to achieve the 256 data transitions.

Figure 2–2 shows the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate equal to 1.25 Gbps.

Figure 2–2. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate Equal to 1.25 Gbps

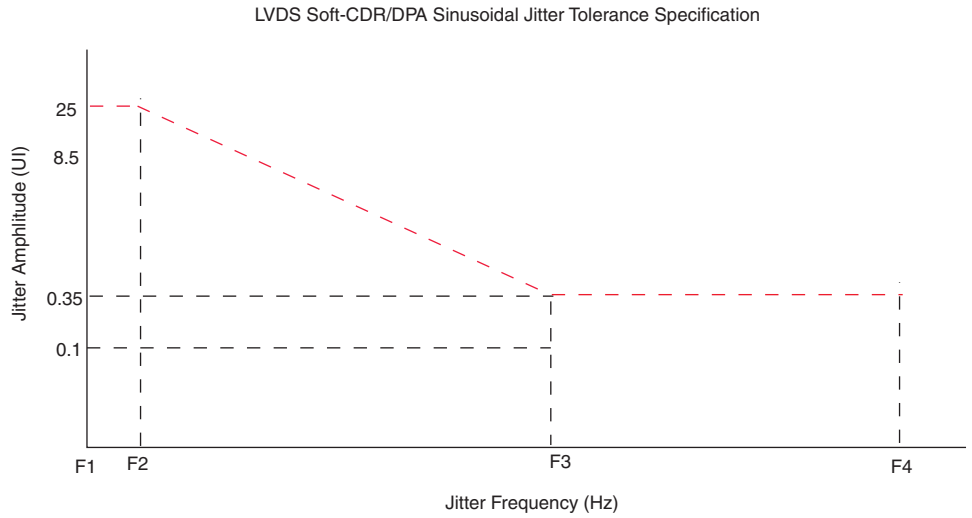


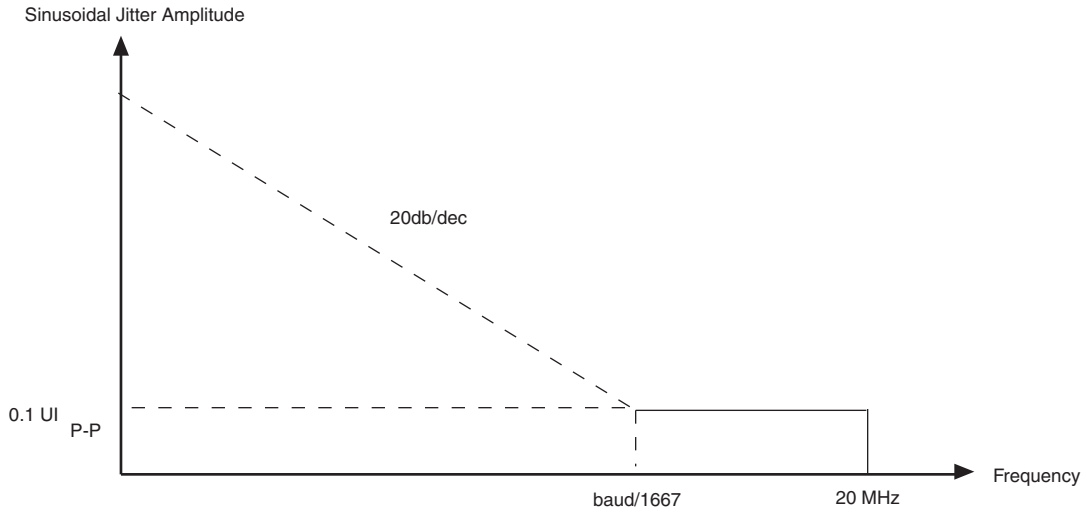
Table 2–31 lists the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate equal to 1.25 Gbps.

Table 2–31. LVDS Soft-CDR/DPA Sinusoidal Jitter Mask Values for a Data Rate Equal to 1.25 Gbps—*Preliminary*

Jitter Frequency (Hz)		Sinusoidal Jitter (UI)
F1	10,000	25.000
F2	17,565	25.000
F3	1,493,000	0.350
F4	50,000,000	0.350

Figure 2–3 shows the LVDS soft-CDR/DPA sinusoidal jitter tolerance specification for a data rate less than 1.25 Gbps.

Figure 2–3. LVDS Soft-CDR/DPA Sinusoidal Jitter Tolerance Specification for a Data Rate Less than 1.25 Gbps



DQS Logic Block and Memory Output Clock Jitter Specifications

Table 2–32 lists the DQS phase shift error for Arria V devices.

Table 2–32. DQS Phase Shift Error Specification for DLL-Delayed Clock (t_{DQS_PSERR}) for Arria V Devices—*Preliminary* (1), (2)

Number of DQS Delay Buffer	–C4 Speed Grade	–C5, I5 Speed Grade	–C6 Speed Grade	Unit
2	57	58	74	ps

Notes to Table 2–32:

(1) The numbers are preliminary pending silicon characterization.

(2) This error specification is the absolute maximum and minimum error. For example, skew on two DQS delay buffers in a –4 speed grade is 58 ps or ±29 ps.

Table 2–33 lists the memory output clock jitter specifications for Arria V devices.

Table 2–33. Memory Output Clock Jitter Specification for Arria V Devices—*Preliminary* (1) (Part 1 of 2)

Parameter	Clock Network	Symbol	–4 Speed Grade		–5 Speed Grade		–6 Speed Grade		Unit
			Min	Max	Min	Max	Min	Max	
Clock period jitter	Regional	$t_{JIT(per)}$	–50	50	–55	55	–55	55	ps
Cycle-to-cycle period jitter	Regional	$t_{JIT(cc)}$	–100	100	–110	110	–110	110	ps
Duty cycle jitter	Regional	$t_{JIT(duty)}$	–50	50	–82.5	82.5	–82.5	82.5	ps
Clock period jitter	Global	$t_{JIT(per)}$	–75	75	–82.5	82.5	–82.5	82.5	ps
Cycle-to-cycle period jitter	Global	$t_{JIT(cc)}$	–150	150	–165	165	–165	165	ps

Table 2–33. Memory Output Clock Jitter Specification for Arria V Devices—*Preliminary* (1) (Part 2 of 2)

Parameter	Clock Network	Symbol	–4 Speed Grade		–5 Speed Grade		–6 Speed Grade		Unit
			Min	Max	Min	Max	Min	Max	
Duty cycle jitter	Global	$t_{JIT(duty)}$	–75	75	–90	90	–90	90	ps

Note to Table 2–33:

(1) The memory output clock jitter measurements are for 200 consecutive clock cycles, as specified in the JEDEC DDR2/DDR3 SDRAM standard.

OCT Calibration Block Specifications

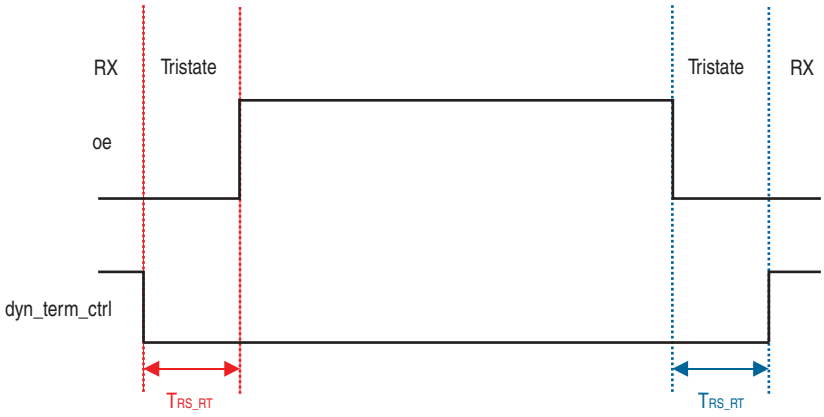
Table 2–34 lists the OCT calibration block specifications for Arria V devices.

Table 2–34. OCT Calibration Block Specifications for Arria V Devices—*Preliminary*

Symbol	Description	Min	Typ	Max	Unit
OCTUSRCLK	Clock required by OCT calibration blocks	—	—	20	MHz
T_{OCTCAL}	Number of OCTUSRCLK clock cycles required for R_S OCT /R_T OCT calibration	—	1000	—	Cycles
$T_{OCTSHIFT}$	Number of OCTUSRCLK clock cycles required for OCT code to shift out	—	32	—	Cycles
T_{RS_RT}	Time required between the `dyn_term_ctrl` and `oe` signal transitions in a bidirectional I/O buffer to dynamically switch between R_S OCT and R_T OCT	—	2.5	—	ns

Figure 2–4 shows the T_{RS_RT} for `dyn_term_ctrl` and `oe` signals.

Figure 2–4. Timing Diagram for dyn_term_ctrl and oe Signals



Duty Cycle Distortion (DCD) Specifications

Table 2–35 lists the worst-case DCD for Arria V devices.

Table 2–35. Worst-Case DCD on Arria V I/O Pins—*Preliminary*

Symbol	–C4 Speed Grade		–C5,I5 Speed Grade		–C6 Speed Grade		Unit
	Min	Max	Min	Max	Min	Max	
Output Duty Cycle	45	55	45	55	45	55	%

Configuration Specification

This section provides configuration specifications and timing for Arria V devices.

These characteristics can be designated as Preliminary or Final.

- Preliminary characteristics are created using simulation results, process data, and other known parameters. The title of these tables show the designation as "Preliminary."
- Final numbers are based on actual silicon characterization and testing. The numbers reflect the actual performance of the device under worst-case silicon process, voltage, and junction temperature conditions. There are no designations on finalized tables.

POR Specifications

Table 2–36 lists the specifications for fast and standard POR for Arria V devices.

Table 2–36. Fast and Standard POR Delay Specification for Arria V Devices (1)

POR Delay	Minimum (ms)	Maximum (ms)
Fast (2)	4	12
Standard (3)	100	300

Notes to Table 2–36:

(1) Select the POR delay based on the MSEL setting as described in the "Configuration Schemes for Arria V Devices" table in the *Configuration, Design Security, and Remote System Upgrades in Arria V Devices* chapter.

(2) When the PORSEL signal is **high**, the device is in fast POR delay.

(3) When the PORSEL signal is **low**, the device is in standard POR delay.

JTAG Configuration Timing

Table 2–37 lists the JTAG timing parameters and values for Arria V devices.

Table 2–37. JTAG Timing Parameters and Values for Arria V Devices—*Preliminary* (Part 1 of 2)

Symbol	Description	Min	Max	Unit
t_{JCP}	TCK clock period	30	—	ns
t_{JCH}	TCK clock high time	14	—	ns
t_{JCL}	TCK clock low time	14	—	ns
$t_{JPSU\ (TDI)}$	TDI JTAG port setup time	1	—	ns

Table 2–37. JTAG Timing Parameters and Values for Arria V Devices—*Preliminary* (Part 2 of 2)

Symbol	Description	Min	Max	Unit
$t_{JPSU\ (TMS)}$	TMS JTAG port setup time	3	—	ns
t_{JPH}	JTAG port hold time	5	—	ns
t_{JPCO}	JTAG port clock to output	—	11 (1)	ns
t_{JPZX}	JTAG port high impedance to valid output	—	14 (1)	ns
t_{JPXZ}	JTAG port valid output to high impedance	—	14 (1)	ns

Note to Table 2–37:

(1) A 1-ns adder is required for each V_{CCIO} voltage step down from 3.0 V. For example, t_{JPCO} = 12 ns if V_{CCIO} of the TDO I/O bank = 2.5 V, or 13 ns if it equals 1.8 V.

FPP Configuration Timing

This section describes the fast passive parallel (FPP) configuration timing parameters for Arria V devices.

DCLK-to-DATA[] Ratio (r) for FPP Configuration

FPP configuration requires a different DCLK-to-DATA[] ratio when you turn on encryption or the compression feature.

Table 2–38 lists the DCLK-to-DATA[] ratio for each combination.

Table 2–38. DCLK-to-DATA[] Ratio for Arria V Devices (1)

Configuration Scheme	Encryption	Compression	DCLK-to-DATA[] ratio (r)
FPP (8-bit wide)	Off	Off	1
	On	Off	1
	Off	On	2
	On	On	2
FPP (16-bit wide)	Off	Off	1
	On	Off	2
	Off	On	4
	On	On	4

Note to Table 2–38:

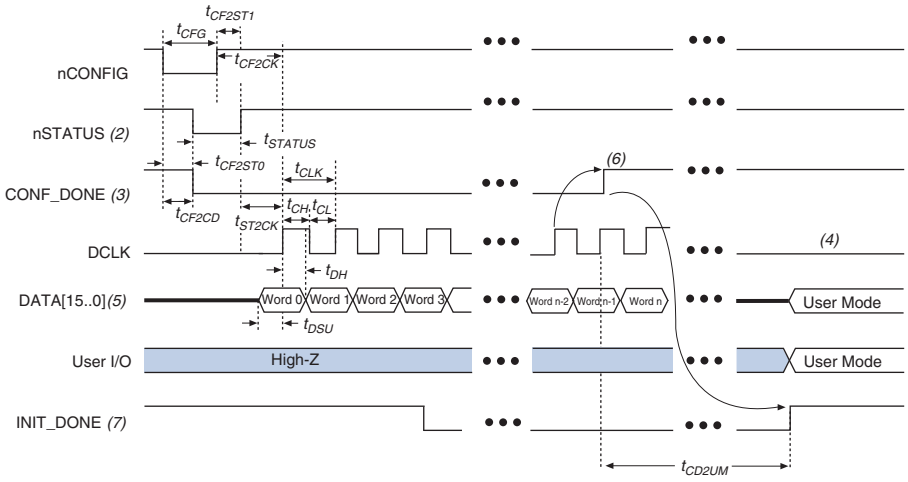
(1) Depending on the DCLK-to-DATA[] ratio, the host must send a DCLK frequency that is r times the DATA[] rate in byte per second (Bps) or word per second (Wps). For example, in FPP x16 where the r is 2, the DCLK frequency must be 2 times the DATA[] rate in Wps.

FPP Configuration Timing when DCLK to DATA[] = 1

Figure 2–5 shows the timing waveform for a FPP configuration when using a MAX® II device as an external host. This timing waveform shows timing when the DCLK-to-DATA[] ratio is 1.

When you enable decompression or the design security feature, the DCLK-to-DATA[] ratio varies for FPP x8 and FPP x16. For the respective DCLK-to-DATA[] ratio, refer to Table 2–38.

Figure 2–5. DCLK-to-DATA[] FPP Configuration Timing Waveform When the Ratio is 1 *(1)*



Notes to Figure 2–5:

(1) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic-high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.

(2) After power up, the Arria V device holds nSTATUS low for the time of the POR delay.

(3) After power up, before and during configuration, CONF_DONE is low.

(4) Do not leave DCLK floating after configuration. You can drive it high or low, whichever is more convenient.

(5) For FPP x16, use DATA[15..0]. For FPP x8, use DATA[7..0]. DATA[15..0] are available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings.

(6) To ensure a successful configuration, send the entire configuration data to the Arria V device. CONF_DONE is released high when the Arria V device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.

(7) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Table 2–39 lists the timing parameters for Arria V devices for FPP configuration when the DCLK-to-DATA[] ratio is 1.

Table 2–39. DCLK-to-DATA[] FPP Timing Parameters for Arria V Devices When the Ratio is 1—*Preliminary* *(1)* (Part 1 of 2)

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	1506 *(2)*	µs

Table 2–39. DCLK-to-DATA[] FPP Timing Parameters for Arria V Devices When the Ratio is 1—*Preliminary* (1) (Part 2 of 2)

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1506 (3)	µs
t_{CF2CK}	nCONFIG high to first rising edge on DCLK	1506	—	µs
t_{ST2CK}	nSTATUS high to first rising edge of DCLK	2	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	0.45 x $1/f_{MAX}$	—	ns
t_{CL}	DCLK low time	0.45 x $1/f_{MAX}$	—	ns
t_{CLK}	DCLK period	$1/f_{MAX}$	—	ns
f_{MAX}	DCLK frequency (FPP x8/ x16)	—	125	MHz
t_R	Input rise time	—	40	ns
t_F	Input fall time	—	40	ns
t_{CD2UM}	CONF_DONE high to user mode (4)	175	437	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (T_{init} x CLKUSR period)	—	—
T_{init}	Number of clock cycles required for device initialization	17,408	—	Cycles

Notes to Table 2–39:

(1) Use these timing parameters when the DCLK-to-DATA[] ratio is 1. To find the DCLK-to-DATA[] ratio for your system, refer Table 2–38 on page 2–37.

(2) You can obtain this value if you do not delay configuration by extending the nCONFIG or the nSTATUS low pulse width.

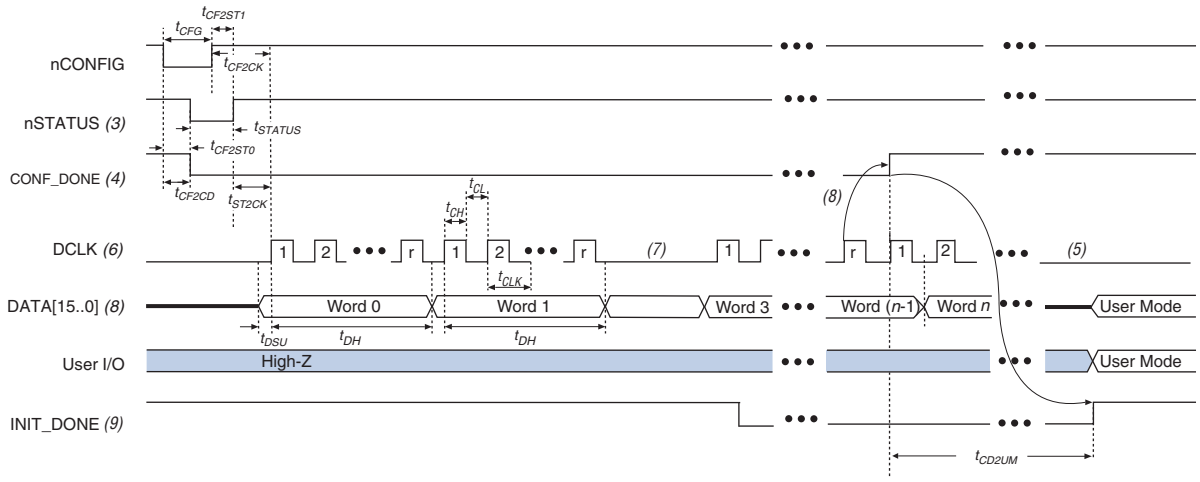
(3) You can obtain this value if you do not delay configuration by externally holding the nSTATUS low.

(4) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

FPP Configuration Timing when DCLK to DATA[] > 1

Figure 2–6 shows the timing waveform for a FPP configuration when using a MAX II device or microprocessor as an external host. This waveform shows timing when the DCLK-to-DATA[] ratio is more than 1.

Figure 2–6. FPP Configuration Timing Waveform When the DCLK-to-DATA[] Ratio is >1 *(1), (2)*



Notes to Figure 2–6:

(1) To find the DCLK-to-DATA[] ratio for your system, refer Table 2–38 on page 2–37.

(2) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.

(3) After power up, the Arria V device holds nSTATUS low for the time as specified by the POR delay.

(4) After power up, before and during configuration, CONF_DONE is low.

(5) Do not leave DCLK floating after configuration. You can drive it high or low, whichever is more convenient.

(6) "r" denotes the DCLK-to-DATA[] ratio. For the DCLK-to-DATA[] ratio based on the decompression and the design security feature enable settings, refer to Table 2–38 on page 2–37.

(7) If needed, pause DCLK by holding it low. When DCLK restarts, the external host must provide data on the DATA[15..0] pins prior to sending the first DCLK rising edge.

(8) To ensure a successful configuration, send the entire configuration data to the Arria V device. CONF_DONE is released high after the Arria V device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.

(9) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Table 2–40 lists the timing parameters for Arria V devices when the DCLK-to-DATA[] ratio is more than 1.

Table 2–40. DCLK-to-DATA[] FPP Timing Parameters for Arria V Devices When the Ratio is >1—*Preliminary*(1)

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	1506 (2)	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1506 (3)	µs
t_{CF2CK}	nCONFIG high to first rising edge on DCLK	1506	—	µs
t_{ST2CK}	nSTATUS high to first rising edge of DCLK	2	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	3 x $1/f_{DCLK}$	—	ns
t_{CH}	DCLK high time	0.45 x $1/f_{MAX}$	—	ns
t_{CL}	DCLK low time	0.45 x $1/f_{MAX}$	—	ns
t_{CLK}	DCLK period	$1/f_{MAX}$	—	ns
f_{MAX}	DCLK frequency (FPP x8/ x16)	—	125	MHz
t_R	Input rise time	—	40	ns
t_F	Input fall time	—	40	ns
t_{CD2UM}	CONF_DONE high to user mode (4)	175	437	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 × maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (T_{init} x CLKUSR period)	—	—
T_{init}	Number of clock cycles required for device initialization	17,408	—	Cycles

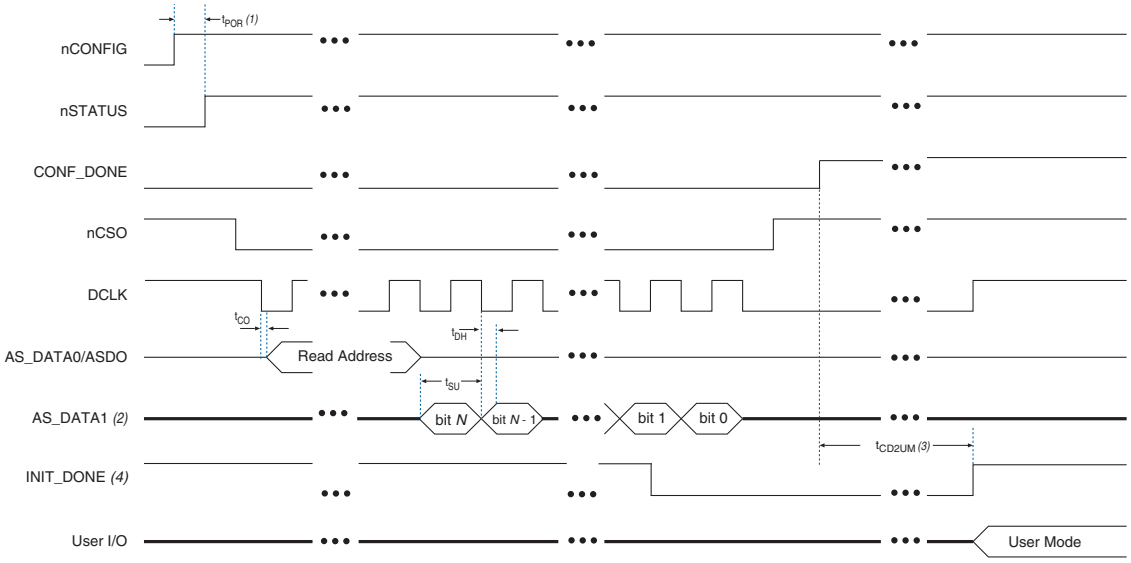
Notes to Table 2–40:

(1) Use these timing parameters when you use decompression and the design security features.
(2) This value can be obtained if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.
(3) This value can be obtained if you do not delay configuration by externally holding nSTATUS low.
(4) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

AS Configuration Timing

Figure 2–7 shows the timing waveform for the active serial (AS) x1 mode and AS x4 mode configuration timing.

Figure 2–7. AS Configuration Timing



Notes to Figure 2–7:

(1) The AS scheme supports standard and fast POR delay (t_{POR}). For t_{POR} delay information, refer to the "POR Delay Specification" section in the *Configuration, Design Security, and remote System Upgrades in Arria V Devices* chapter.

(2) If you are using AS x4 mode, this signal represents the AS_DATA[3..0] and EPCQ sends in 4-bits of data for each DCLK cycle.

(3) The initialization clock can be from the internal oscillator or CLKUSR pin.

(4) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Table 2–41 lists the timing parameters for AS x1 and AS x4 configurations in Arria V devices.

Table 2–41. AS Timing Parameters for AS x1 and x4 Configurations in Arria V Devices—*Preliminary* (1), (2)

Symbol	Parameter	Minimum	Maximum	Unit
t_{CO}	DCLK falling edge to the AS_DATA0/ASDO output	—	4	µs
t_{SU}	Data setup time before the rising edge on DCLK	1.5	—	ns
t_H	Data hold time after the rising edge on DCLK	0	—	ns
t_{CD2UM}	CONF_DONE high to user mode	175	437	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 x maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (T_{init} x CLKUSR period)	—	—
T_{init}	Number of clock cycles required for device initialization	17,408	—	Cycles

Notes to Table 2–41:

(1) The minimum and maximum numbers apply only if you choose the internal oscillator as the clock source for initializing the device.

(2) The t_{CF2CD}, t_{CF2ST0}, t_{CFG}, t_{STATUS}, and t_{CF2ST1} timing parameters are identical to the timing parameters for PS mode listed in Table 2–43 on page 2–44.

Table 2–42 lists the internal clock frequency specification for the AS configuration scheme.

Table 2–42. DCLK Frequency Specification in the AS Configuration Scheme—*Preliminary* (1), (2)

Minimum	Typical	Maximum	Unit
5.3	7.9	12.5	MHz
10.6	15.7	25.0	MHz
21.3	31.4	50.0	MHz
42.6	62.9	100.0	MHz

Notes to Table 2–42:

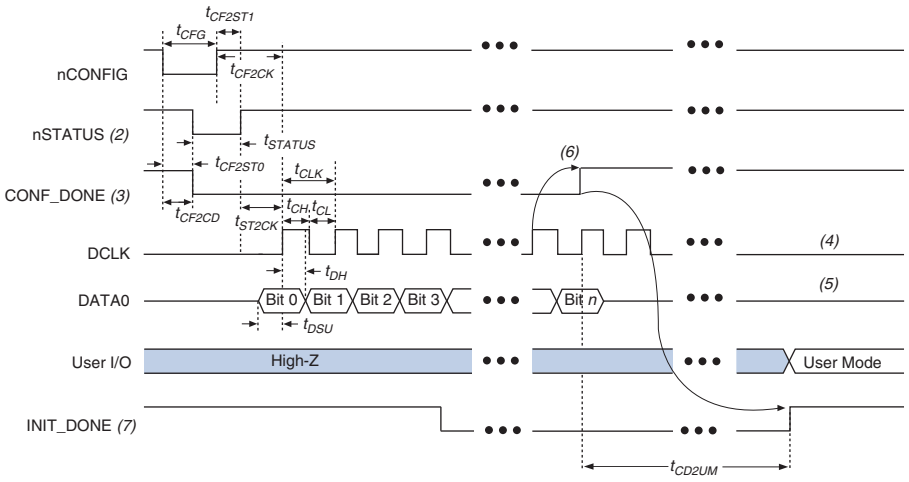
(1) This applies to the DCLK frequency specification when using the internal oscillator as the configuration clock source.

(2) The AS multi-device configuration scheme does not support DCLK frequency of 100 MHz.

PS Configuration Timing

Figure 2–8 shows the timing waveform for a passive serial (PS) configuration when using a MAX II device or microprocessor as an external host.

Figure 2–8. PS Configuration Timing Waveform (1)



Notes to Figure 2–8:

(1) The beginning of this waveform shows the device in user mode. In user mode, nCONFIG, nSTATUS, and CONF_DONE are at logic high levels. When nCONFIG is pulled low, a reconfiguration cycle begins.

(2) After power up, the Arria V device holds nSTATUS low for the time of the POR delay.

(3) After power up, before and during configuration, CONF_DONE is low.

(4) Do not leave DCLK floating after configuration. You can drive it high or low, whichever is more convenient.

(5) DATA0 is available as a user I/O pin after configuration. The state of this pin depends on the dual-purpose pin settings in the **Device and Pins Option**.

(6) To ensure a successful configuration, send the entire configuration data to the Arria V device. CONF_DONE is released high after the Arria V device receives all the configuration data successfully. After CONF_DONE goes high, send two additional falling edges on DCLK to begin initialization and enter user mode.

(7) After the option bit to enable the INIT_DONE pin is configured into the device, the INIT_DONE goes low.

Table 2–43 lists the PS timing parameter for Arria V devices.

Table 2–43. PS Timing Parameters for Arria V Devices—*Preliminary*

Symbol	Parameter	Minimum	Maximum	Unit
t_{CF2CD}	nCONFIG low to CONF_DONE low	—	600	ns
t_{CF2ST0}	nCONFIG low to nSTATUS low	—	600	ns
t_{CFG}	nCONFIG low pulse width	2	—	µs
t_{STATUS}	nSTATUS low pulse width	268	1506 (1)	µs
t_{CF2ST1}	nCONFIG high to nSTATUS high	—	1506 (2)	µs
t_{CF2CK}	nCONFIG high to first rising edge on DCLK	1506	—	µs
t_{ST2CK}	nSTATUS high to first rising edge of DCLK	2	—	µs
t_{DSU}	DATA[] setup time before rising edge on DCLK	5.5	—	ns
t_{DH}	DATA[] hold time after rising edge on DCLK	0	—	ns
t_{CH}	DCLK high time	0.45 x $1/f_{MAX}$	—	ns
t_{CL}	DCLK low time	0.45 x $1/f_{MAX}$	—	ns
t_{CLK}	DCLK period	$1/f_{MAX}$	—	ns
f_{MAX}	DCLK frequency	—	125	MHz
t_R	Input rise time	—	40	ns
t_F	Input fall time	—	40	ns
t_{CD2UM}	CONF_DONE high to user mode (3)	175	437	µs
t_{CD2CU}	CONF_DONE high to CLKUSR enabled	4 x maximum DCLK period	—	—
t_{CD2UMC}	CONF_DONE high to user mode with CLKUSR option on	t_{CD2CU} + (T_{init} x CLKUSR period)	—	—
T_{init}	Number of clock cycles required for device initialization	17,408	—	Cycles

Notes to Table 2–43:

(1) You can obtain this value if you do not delay configuration by extending the nCONFIG or nSTATUS low pulse width.

(2) You can obtain this value if you do not delay configuration by externally holding nSTATUS low.

(3) The minimum and maximum numbers apply only if you chose the internal oscillator as the clock source for initializing the device.

Remote System Upgrades Circuitry Timing Specification

Table 2–44 lists the timing parameter specifications for the remote system upgrade circuitry.

Table 2–44. Remote System Upgrade Circuitry Timing Specification

Parameter	Minimum	Maximum	Unit
$t_{MAX\_RU\_CLK}$ (1)	—	40	MHz
$t_{RU\_nCONFIG}$ (2)	250	—	ns
$t_{RU\_nRSTIMER}$ (3)	250	—	ns

Notes to Table 2–44:

(1) This clock is user-supplied to the remote system upgrade circuitry. If you are using the ALTREMOTE_UPDATE megafunction, the clock user-supplied to the ALTREMOTE_UPDATE megafunction must meet this specification.

(2) This is equivalent to strobing the reconfiguration input of the ALTREMOTE_UPDATE megafunction high for the minimum timing specification. For more information, refer to the "Remote System Upgrade State Machine" section in the *Device Interfaces and Integration Basics for Arria V Devices* chapter.

(3) This is equivalent to strobing the reset timer input of the ALTREMOTE_UPDATE megafunction high for the minimum timing specification. For more information, refer to the "User Watchdog Timer" section in the *Device Interfaces and Integration Basics for Arria V Devices* chapter.

User Watchdog Internal Oscillator Frequency Specification

Table 2–45 lists the frequency specifications for the user watchdog internal oscillator.

Table 2–45. User Watchdog Internal Oscillator Frequency Specifications—*Preliminary*

Minimum	Typical	Maximum	Unit
5.3	7.9	12.5	MHz

I/O Timing

Altera offers two ways to determine I/O timing—the Excel-based I/O Timing and the Quartus II Timing Analyzer.

Excel-based I/O timing provides pin timing performance for each device density and speed grade. The data is typically used prior to designing the FPGA to get an estimate of the timing budget as part of the link timing analysis. The Quartus II Timing Analyzer provides a more accurate and precise I/O timing data based on the specifics of the design after you complete place-and-route.

You can download the Excel-based I/O Timing spreadsheet from the Arria V Devices Literature webpage.

Programmable IOE Delay

Table 2–46 lists the Arria V IOE programmable delay settings.

Table 2–46. IOE Programmable Delay for Arria V Devices *(1)*

Parameter	Available Settings	Minimum Offset	Fast Model		Slow Model			Unit
			Industrial	Commercial	C4	C5, I5	C6	
TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns
TBD	TBD	TBD	TBD	TBD	TBD	TBD	TBD	ns

Note to Table 2–46:

(1) Pending the Quartus II software extraction.

Programmable Output Buffer Delay

Table 2–47 lists the delay chain settings that control the rising and falling edge delays of the output buffer. The default delay is 0 ps.

Table 2–47. Programmable Output Buffer Delay—*Preliminary* *(1), (2)*

Symbol	Parameter	Typical	Unit
D_{OUTBUF}	Rising and/or falling edge delay	0 (default)	ps
		50	ps
		100	ps
		150	ps

Notes to Table 2–47:

(1) Pending the Quartus II software extraction.

(2) You can set the programmable output buffer delay in the Quartus II software by setting the **Output Buffer Delay Control** assignment to either positive, negative, or both edges, with the specific values stated here (in ps) for the **Output Buffer Delay** assignment.

Glossary

Table 2–48 lists the glossary for this chapter.

Table 2–48. Glossary Table (Part 1 of 4)

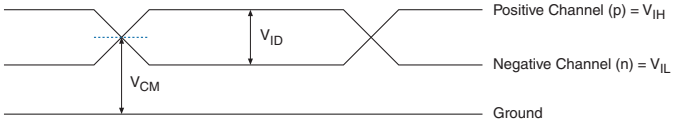
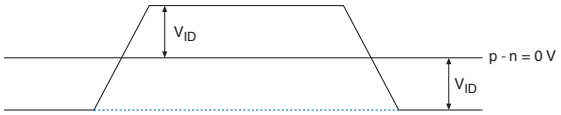
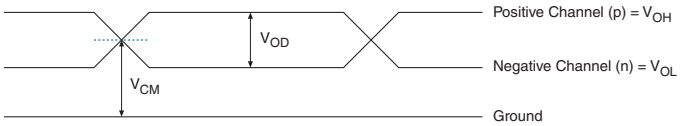
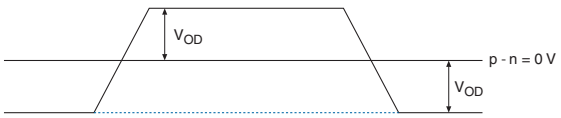
Letter	Subject	Definitions
A B C	—	—
D	Differential I/O Standards	*Receiver Input Waveforms* **Single-Ended Waveform**  **Differential Waveform**  *Transmitter Output Waveforms* **Single-Ended Waveform**  **Differential Waveform** 
E	—	—
F	f_{HSCLK}	Left/right PLL input clock frequency.
	f_{HSDR}	High-speed I/O block—Maximum/minimum LVDS data transfer rate (f_{HSDR} = 1/TUI), non-DPA.
	$f_{HSDRDPA}$	High-speed I/O block—Maximum/minimum LVDS data transfer rate ($f_{HSDRDPA}$ = 1/TUI), DPA.
G H I	—	—

Table 2–48. Glossary Table (Part 2 of 4)

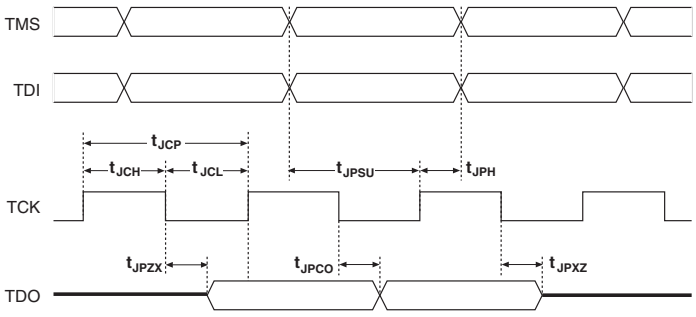
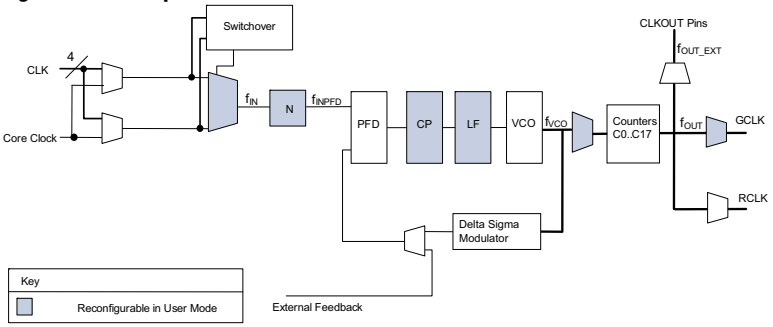
Letter	Subject	Definitions
J	J	High-speed I/O block—Deserialization factor (width of parallel data bus).
J	JTAG Timing Specifications	JTAG Timing Specifications: 
K L M N O	—	—
P	**PLL Specifications**	**Diagram of PLL Specifications** *(1)*  **Note:** (1) `Core Clock` can only be fed by dedicated clock input pins or PLL outputs.
Q	—	—
R	R_L	Receiver differential input discrete resistor (external to the Arria V device).

Table 2–48. Glossary Table (Part 3 of 4)

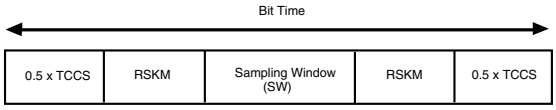
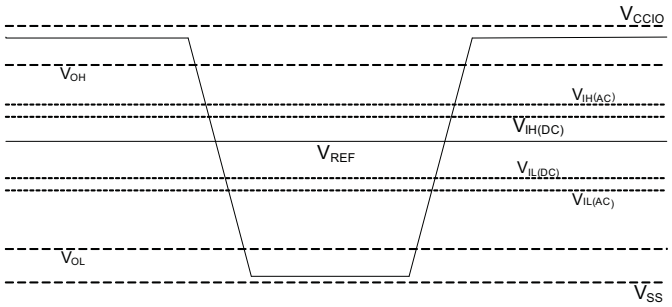
Letter	Subject	Definitions
S	**Sampling window (SW)**	Timing Diagram—the period of time during which the data must be valid in order to capture it correctly. The setup and hold times determine the ideal strobe position in the sampling window, as shown: 
	Single-ended voltage referenced I/O standard	The JEDEC standard for the SSTI and HSTL I/O defines both the AC and DC input signal values. The AC values indicate the voltage levels at which the receiver must meet its timing specifications. The DC values indicate the voltage levels at which the final logic state of the receiver is unambiguously defined. After the receiver input has crossed the AC value, the receiver changes to the new logic state. The new logic state is then maintained as long as the input stays beyond the AC threshold. This approach is intended to provide predictable receiver timing in the presence of input waveform ringing, as shown: *Single-Ended Voltage Referenced I/O Standard* 
T	t_C	High-speed receiver/transmitter input and output clock period.
	TCCS (channel-to-channel-skew)	The timing difference between the fastest and slowest output edges, including the t_{CO} variation and clock skew, across channels driven by the same PLL. The clock is included in the TCCS measurement (refer to the *Timing Diagram* figure under **SW** in this table).
	t_{DUTY}	High-speed I/O block—Duty cycle on high-speed transmitter output clock.
		Timing Unit Interval (TUI) The timing budget allowed for skew, propagation delays, and the data sampling window. (TUI = 1/(Receiver Input Clock Frequency Multiplication Factor) = t_C/w)
	t_{FALL}	Signal high-to-low transition time (80–20%)
	t_{INCCJ}	Cycle-to-cycle jitter tolerance on the PLL clock input
	t_{OUTPJ_IO}	Period jitter on the GPIO driven by a PLL
	t_{OUTPJ_DC}	Period jitter on the dedicated clock output driven by a PLL
	t_{RISE}	Signal low-to-high transition time (20–80%)
U	—	—

Table 2–48. Glossary Table (Part 4 of 4)

Letter	Subject	Definitions
V	$V_{CM(DC)}$	DC Common mode input voltage.
	V_{ICM}	Input Common mode voltage—The common mode of the differential signal at the receiver.
	V_{ID}	Input differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the receiver.
	$V_{DIF(AC)}$	AC differential input voltage—Minimum AC input differential voltage required for switching.
	$V_{DIF(DC)}$	DC differential input voltage— Minimum DC input differential voltage required for switching.
	V_{IH}	Voltage input high—The minimum positive voltage applied to the input which is accepted by the device as a logic high.
	$V_{IH(AC)}$	High-level AC input voltage
	$V_{IH(DC)}$	High-level DC input voltage
	V_{IL}	Voltage input low—The maximum positive voltage applied to the input which is accepted by the device as a logic low.
	$V_{IL(AC)}$	Low-level AC input voltage
	$V_{IL(DC)}$	Low-level DC input voltage
	V_{OCM}	Output Common mode voltage—The common mode of the differential signal at the transmitter.
	V_{OD}	Output differential voltage swing—The difference in voltage between the positive and complementary conductors of a differential transmission at the transmitter.
	V_{SWING}	Differential input voltage
	V_X	Input differential cross point voltage
	V_{OX}	Output differential cross point voltage
W	W	High-speed I/O block—Clock Boost Factor
X, Y, Z	—	—

Document Revision History

Table 2–49 lists the revision history for this chapter.

Table 2–49. Document Revision History

Date	Version	Changes
November. 2011	1.1	■ Updated Table 2–1, Table 2–19, Table 2–26, and Table 2–36. ■ Added Table 2–5. ■ Added Figure 2–4.
August 2011	1.0	Initial release.

This chapter provides additional information about the document and Altera.

How to Contact Altera

To locate the most up-to-date information about Altera products, refer to the following table.

Contact (1)	Contact Method	Address
Technical support	Website	www.altera.com/support
Technical training	Website	www.altera.com/training
	Email	custrain@altera.com
Product literature	Website	www.altera.com/literature
Nontechnical support (general)	Email	nacomp@altera.com
(software licensing)	Email	authorization@altera.com

Note to Table:

(1) You can also contact your local Altera sales office or sales representative.

Typographic Conventions

The following table shows the typographic conventions this document uses.

Visual Cue	Meaning
Bold Type with Initial Capital Letters	Indicate command names, dialog box titles, dialog box options, and other GUI labels. For example, **Save As** dialog box. For GUI elements, capitalization matches the GUI.
bold type	Indicates directory names, project names, disk drive names, file names, file name extensions, software utility names, and GUI labels. For example, **\qdesigns** directory, **D:** drive, and **chiptrip.gdf** file.
Italic Type with Initial Capital Letters	Indicate document titles. For example, *Stratix IV Design Guidelines*.
italic type	Indicates variables. For example, *n* + 1. Variable names are enclosed in angle brackets (< >). For example, *<file name>* and *<project name>***.pof** file.
Initial Capital Letters	Indicate keyboard keys and menu names. For example, the Delete key and the Options menu.
"Subheading Title"	Quotation marks indicate references to sections in a document and titles of Quartus II Help topics. For example, "Typographic Conventions."

Visual Cue	Meaning
Courier type	Indicates signal, port, register, bit, block, and primitive names. For example, `data1`, `tdi`, and `input`. The suffix `n` denotes an active-low signal. For example, `resetn`. Indicates command line commands and anything that must be typed exactly as it appears. For example, `c:\qdesigns\tutorial\chiptrip.gdf`. Also indicates sections of an actual file, such as a Report File, references to parts of files (for example, the AHDL keyword `SUBDESIGN`), and logic function names (for example, `TRI`).
↵	An angled arrow instructs you to press the Enter key.
1., 2., 3., and a., b., c., and so on	Numbered steps indicate a list of items when the sequence of the items is important, such as the steps listed in a procedure.
■ ■ ■	Bullets indicate a list of items when the sequence of the items is not important.
	The hand points to information that requires special attention.
	A question mark directs you to a software help system with related information.
	The feet direct you to another document or website with related information.
	A caution calls attention to a condition or possible situation that can damage or destroy the product or your work.
	A warning calls attention to a condition or possible situation that can cause you injury.
	The envelope links to the Email Subscription Management Center page of the Altera website, where you can sign up to receive update notifications for Altera documents.